

Introduction to Advanced Low-Voltage Technology

INTRODUCTION

ALVT, Advanced Low-Voltage Technology, provides the designer with a family of very high speed TTL and LVTTTL design options. The selection of devices included in this family allow the engineer to utilize standard bus interface logic functions in speed critical applications. Some features of the ALVT family are:

- Output drive $I_{OH}/I_{OL} = 32/64\text{mA}$ at $V_{CC} = 3.3\text{V}$ and $V_{CC} = 2.5\text{V}$
- Fully I/O compatible from 2.5 to 5.5V
- Output overvoltage protection allows forcing the outputs to 5.5V without additional interfacing. This maintains compatibility with 5V TTL logic without requiring additional components.
- Supports live insertion
- Available in SSOP and TSSOP packaging
- Bus Hold eliminates the need for external pull-up resistors

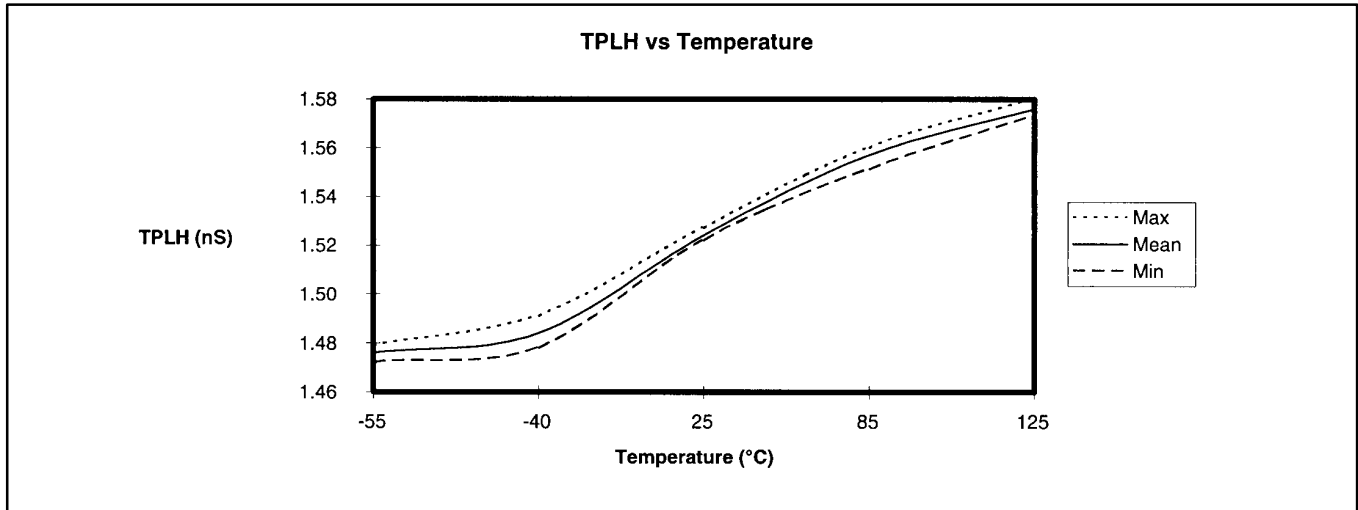


Figure 1.

APPLICATIONS

The ALVT product family offers a number of part types useful in many applications. One such application is driving DRAM arrays.

The variety of 18 and 20 bit devices, coupled with the high drive feature, makes ALVT especially suited for driving large DRAM arrays. In dense DRAM applications, it is useful to buffer CAS, RAS, and address lines through the same part. This reduces the skew

between the individual signals, allowing tighter timing margins. Also, the ALVT162XXX functions feature a 30 ohm series termination resistor on each output. This termination is very effective in reducing the transmission line effects seen in large DRAM arrays. The result of ALVT's high speed, incident wave switching, minimal transmission line effects, and low skew signaling is fast DRAM access in 5V/3.3V TTL or LVTTTL applications.

ALVT16245

t_{PS} (Pin Skew or Transition Skew)

$$t_{PS} = |t_{PHL} - t_{PLH}|$$

	$V_{CC} = 2.3$	$V_{CC} = 2.5$	$V_{CC} = 2.7$	$V_{CC} = 3.0$	$V_{CC} = 3.3$	$V_{CC} = 3.6$
t_{PS} Max (ps)	429	469	430	526	267	336
t_{PS} Min (ps)	39	79	117	73	0	100
t_{PS} Median(ps)	234	274	274	260	97	129

NOTE: One output switching, Temp = 25°C, 9 parts

Another useful application of ALVT is in heavily loaded high bandwidth busses. The high drive of ALVT makes the family a logical choice for use in heavily loaded buses (35-50 ohm). The more popular bus transceiver functions (ALVT162XXX) are available with 30 ohm series output resistors. These resistors help match the impedance of heavily loaded buses, reducing transmission line

induced reflections. Other features supplementing the bus interface application are 5V tolerance on I/Os and LVTTTL switching level compatibility. 5V tolerance on inputs and outputs allows ALVT parts to be connected to 5V TTL or CMOS devices, i.e., a computer bus with 5V interface boards. These features offer flexibility and backward compatibility for use in existing designs.

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PROCESS TECHNOLOGY

The fabrication of ALVT uses an advanced BiCMOS process called QUBiC-LP. This process is a low voltage/low power version of the popular QUBiC process. Some features of QUBiC-LP include:

- 13 GHz bipolar NPN devices
- 0.65µm L_{EFF} CMOS devices
- Complementary temperature characteristics of the bipolar and CMOS devices ensure stable speed performance over temperature
- High impedance, low capacitance (4-5pF) inputs
- Bipolar output structure results in high drive capability
- Lower dynamic power dissipation than competing technologies
- Low V_{CC} and ground bounce

AC CHARACTERISTICS

The most desirable characteristic of ALVT is high speed. This family of logic represents a 20% improvement over LVT devices. This feature coupled with the TTL-LVTTL compatibility makes ALVT a very effective solution in mixed voltage applications. Another desirable AC characteristic is very low pulse skew. The low pulse skew – the difference between t_{PHL} and t_{PLH} – ensures the system designer that a 50% duty cycle input signal will retain the same duty cycle on the output. This makes the designer's timing analysis much easier and results in a tighter system timing.

ALVT is the world's first BiCMOS standard logic family specified for operation in the 2.5V V_{CC} range. At 2.5V, ALVT's speed is

comparable to that of LVT. This coupled with the pin for pin compatibility with LVT allows the system designer to easily migrate existing 3.3V, or even 5V, designs to 2.5V.

INPUT CHARACTERISTICS

ALVT offers both TTL and LVTTTL switching level compatibility. In the 3.3V V_{CC} range TTL switching levels are used, while the 2.5V range switches at LVTTTL levels. The low input capacitance, 4pF per input, along with the low input current requirement results in a high input impedance, a very desirable feature in high fanout situations. The bus hold circuit operates in the 3.3V V_{CC} range, providing pin for pin and feature for feature compatibility with the LVT family. The bus hold circuit shuts down in the 2.5V range, allowing for extra power savings due to reduced input leakage current.

OUTPUT CHARACTERISTICS

The BiCMOS technology used in the design of ALVT enables the IC designer to create very quick, very powerful output structures. The use of the bipolar devices enhances the speed of output switching while the slower CMOS devices provide high output drive. The use of a Philips Semiconductors patented circuit technology called Pass-NMOS BiCMOS Logic enhances the speed of the conventional output structure design. This innovation enables the bipolar devices in the output structure to begin their switching cycle sooner, enabling the fast speeds of ALVT devices.

As shown in Figure 2, the propagation delays of ALVT are very consistent whether switching one output or all sixteen.

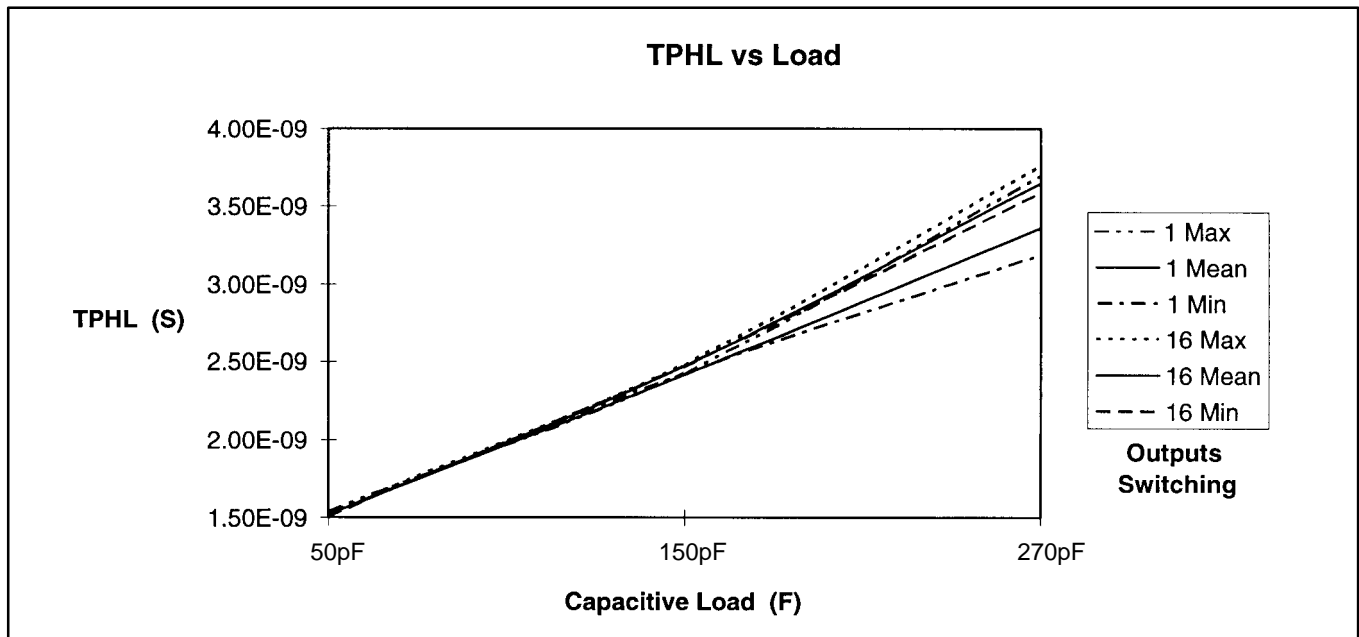


Figure 2.

Another feature of ALVT, live insertion and extraction, is really not a feature anymore, but an industry standard. This feature includes 3-State power-up and reset on power-up. These features combine to

make ALVT an excellent choice in fault-tolerant computer or telecom bus applications.

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POWER DISSIPATION

The primary reason for the push to lower supply voltages revolves around smaller fabrication process geometries. Another important reason is power dissipation on the chip level. From a system point of view, power dissipation at the package and part level are also very

important. The design of the ALVT provides high output drive currents while maximizing overall power consumption.

Figure 3 shows I_{CC} vs frequency with the standard TTL load.

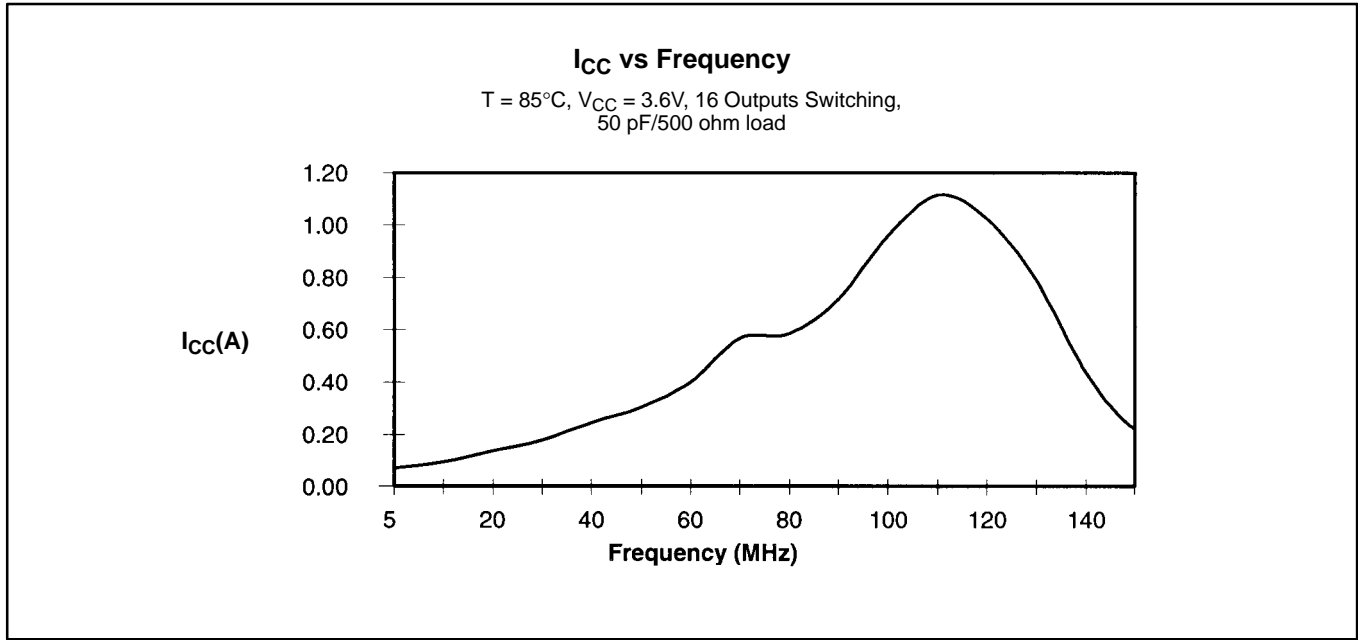


Figure 3.

NOISE

Ground bounce and V_{CC} bounce, also called simultaneous switching noise, are critical sources of noise in logic products. The design of ALVT keeps this fact in mind. The combination of package style, pin configuration, and edge rate control helps keep the effects

of simultaneous switching noise. ALVT attacks this problem through use of SSOP and TSSOP packages, industry standard flow through pinout with multiple ground and V_{CC} pins, and advanced circuit design to actively control edge rates.

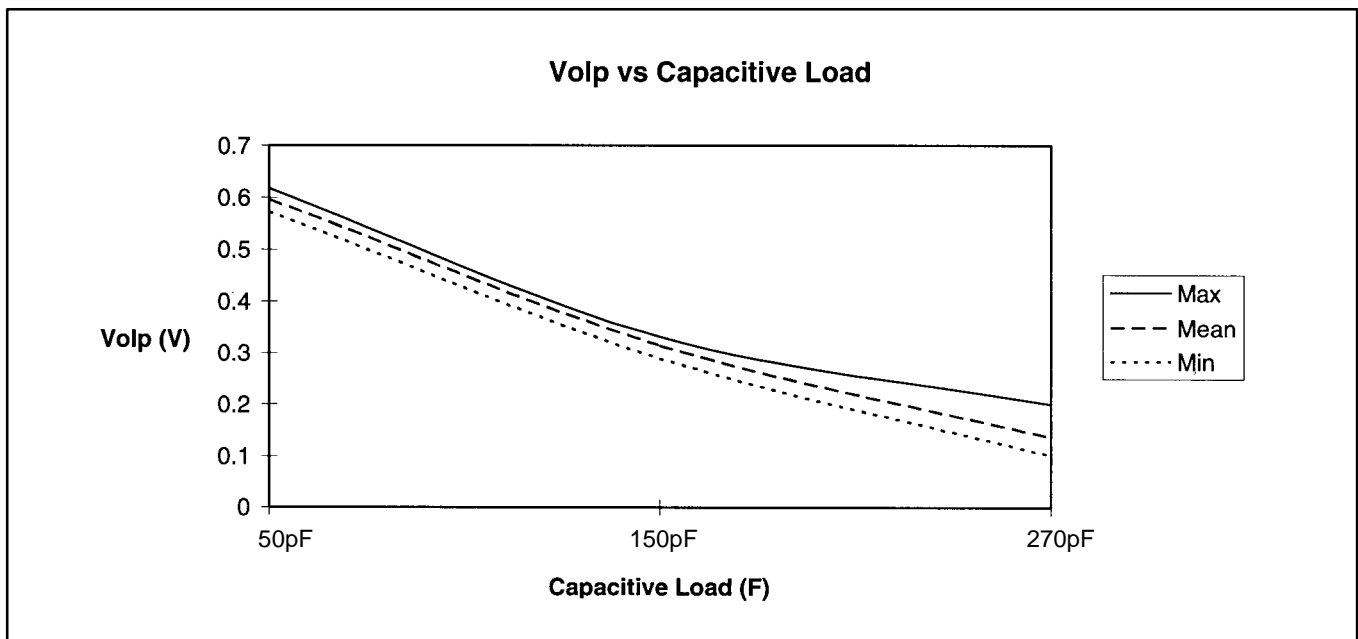


Figure 4.

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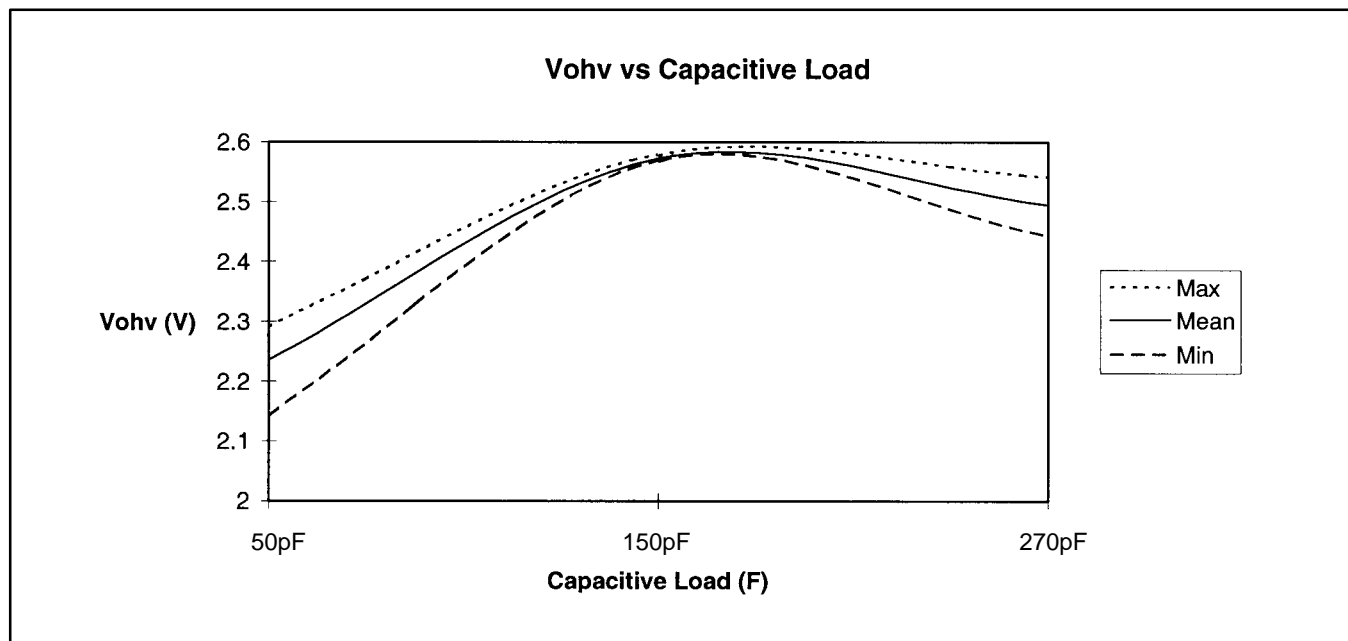


Figure 5.

CONCLUSION

ALVT represents another step in the evolution of standard logic products. The high speed, mixed voltage compatibility, and high drive make the family a superior choice in lower voltage, high speed

CPU designs. The feature set included in the ALVT family and the selection of functions will allow system designers to extend their existing designs well into the future.