

The Philips Logic DQFN package is a small package plastic encapsulate package with a copper lead-frame substrate. The exposed die paddle on the bottom helps to efficiently conduct heat away from the die giving this package about a 15% improvement in thermal power dissipation than the equivalent TSSOP package.

The smaller lead frame and shorter die attach wires also give the package superior electrical characteristics with less ground bounce. This is a leadless package where electrical contact is made by soldering the lands on the bottom surface of the package to the PC board. As shown in figure 1, the lands on the package are rectangular in shape with a rounded edge on the inside. Since this package doesn't have any solder balls or bumps, the electrical connection between the package and the PC board is made by printing the solder paste on the PC and re-flowing it after component placement.

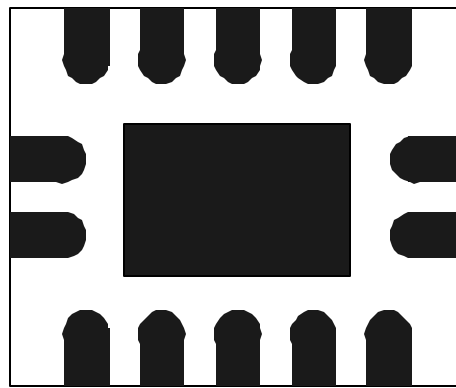


Figure 1. A 14-pad DQFN package

Land pattern design for a solder mask is based on guidelines within a company or by following industry standards such as IPC-SM-782. Since the DQFN package is new to the industry, guidelines specific to this package have not been fully developed. For the purpose of this document, IPC methodology has been followed with special considerations made for the differences unique to this package. All information is preliminary.

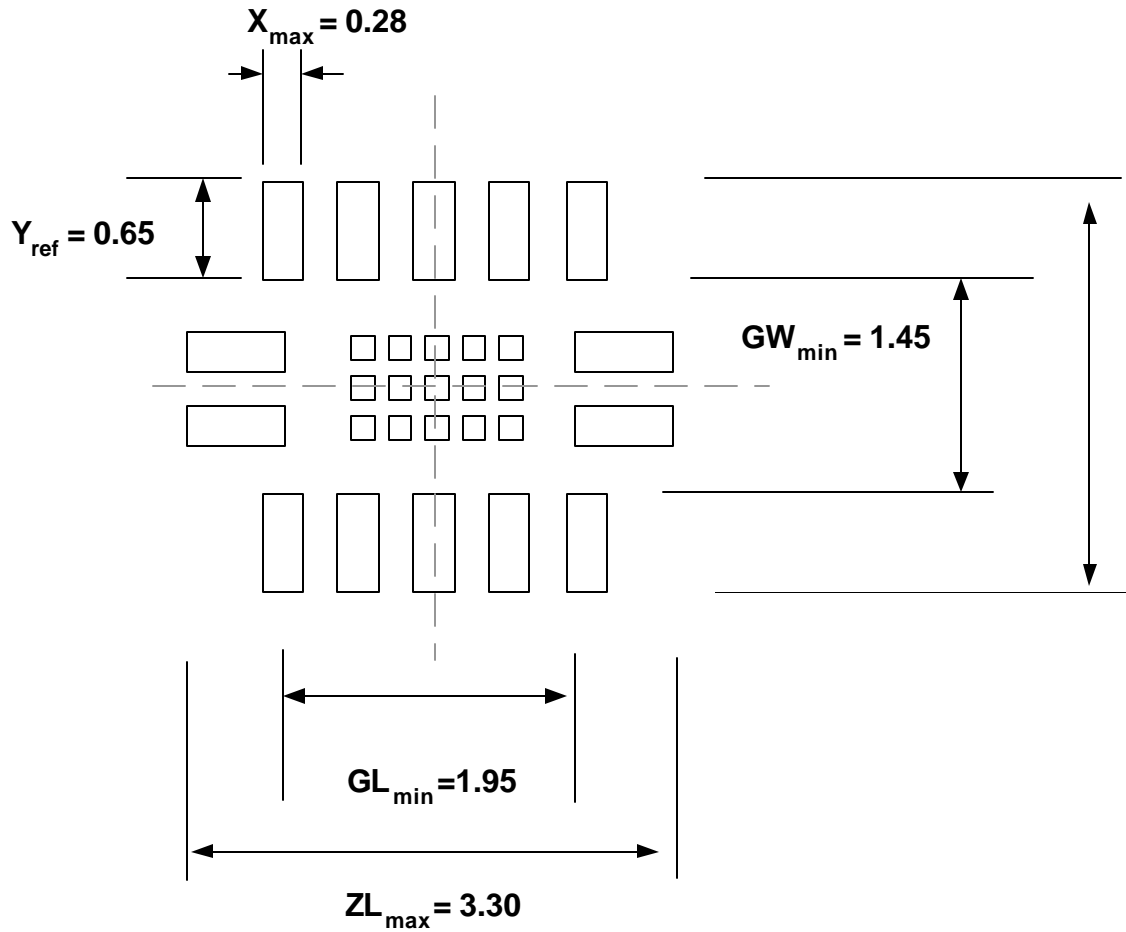


Figure 2. 14 Pad DQFN

Figure 2 is the recommended for the PCB land patterns for the 14-pad device; figures 3 and 4 are for the 16 and 20 pad devices respectively. Thermal pad placement is optional but by using a solder paste pattern of 0.4mm squares to offset the effects of outgassing during reflow. This pattern will typically result in 80% solder paste coverage.

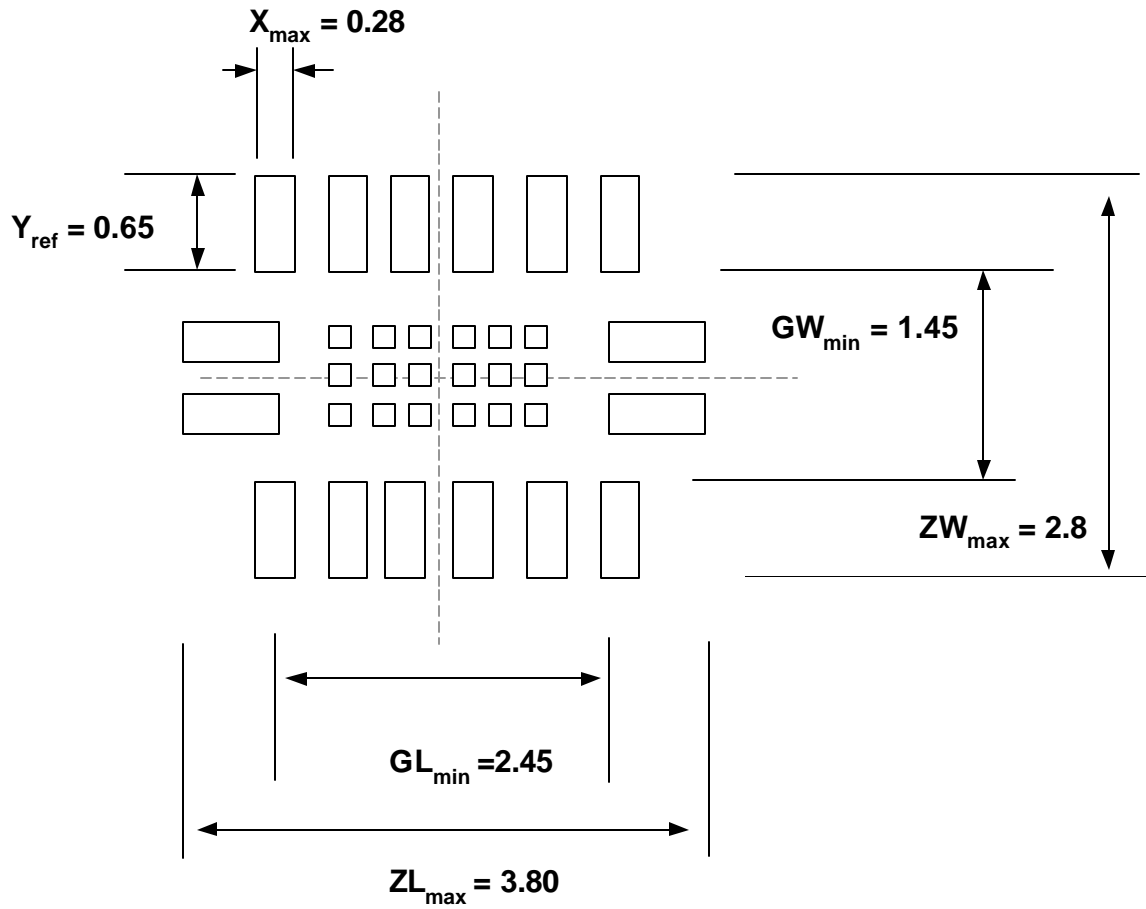


Figure 3. 16 pad DQFN

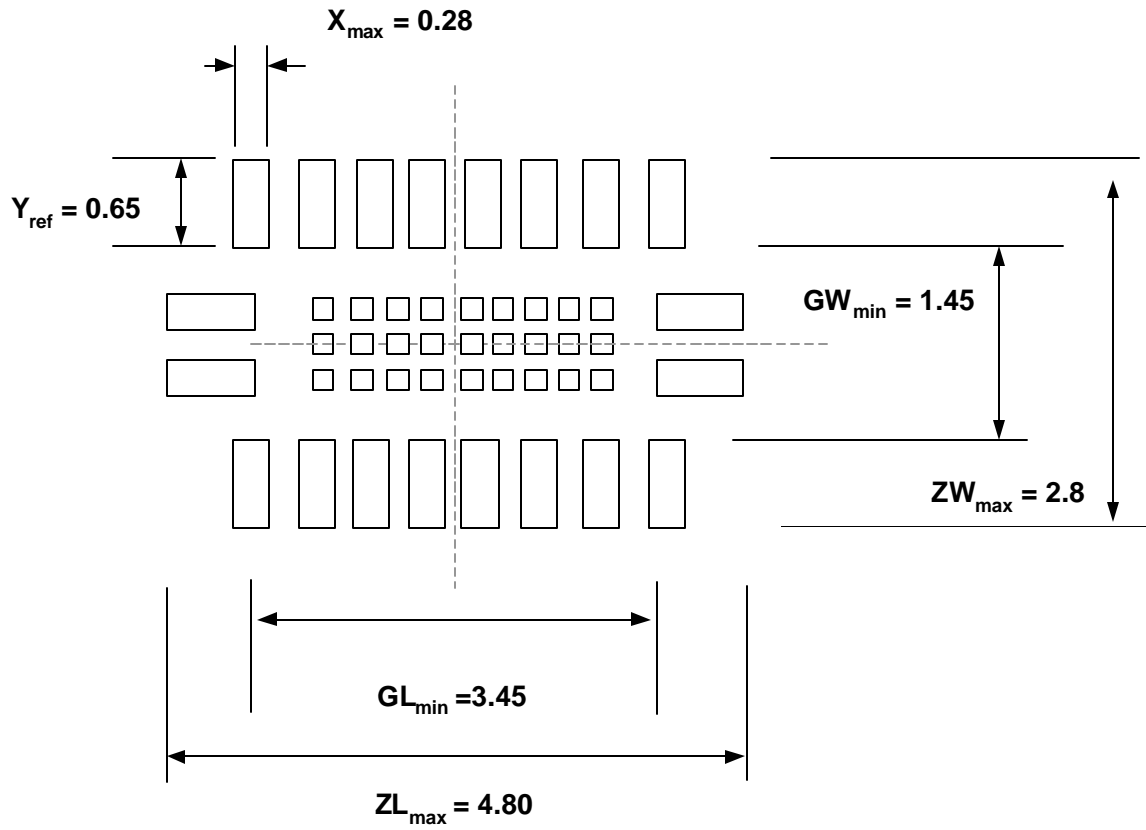


Figure 4: 20 pad DQFN