

APPLICATION NOTE

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PTN products demo board
documentation

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PTN DEMO BOARD

The PTN Demo Board utilizes the following products: PTN1111– a 1:10 PECL Clock distributing device, PTN3311– a PECL to LVDS translator, a PTN2111– a 1:10 LVDS Clock Distributing device, PTN3310– a LVDS to PECL translator, and PTN3322– a universal translator. For more information on the PTN products themselves, please, refer to their corresponding data sheets.

The purpose of the Demo Board is to show the simultaneous operation of all of the above devices, and it is the main mode of operation for the board. However, the board also allows for independent operation for some of the products.

In the main mode of operation, the PTN1111 gets its input signal from a pattern generator via the SMA J6 & SMA J8. One of the PTN1111 outputs goes into the receiver of PTN3311. The output of PTN3311 feeds into one of the clock inputs of PTN2111 if and only if resistors R23 and R24 are assembled. Then, one of the outputs of PTN2111 is fed into the input of the PTN3310, and its outputs are connected to SMA J45 & J7, which could be fed into an oscilloscope. The original signal of this loop is PECL, and the final output signal is also PECL after it has been translated to and then again from LVDS.

The PTN3322 could provide an input to either the PTN1111 or the PTN2111, as selected by the L/P pin of Switch 1. If the PTN3322 is to drive the PTN1111, resistors R13 and R14 must be soldered to the board, and then the PTN3322 becomes the default source of the main loop. The PTN1111's clock select pin, Clk_Sel, on Switch 2 must be in open position. Alternatively, if the PTN3322 is to be a signaling source for the PTN2111, the Si pin of Switch 1 must be in an open position.

The PTN3322 could be evaluated by itself. LVDS signal levels can be applied via SMA J3 and SMA J4, and then resistors R11 and R12 must be assembled, so PTN3322's outputs are connected to SMA J1 and SMA J2 (R13 and R14 should be dismantled). If the PECL outputs should be evaluated, then the corresponding PECL terminations should be assembled, namely, resistors R7, R8, R9, and R10. If the LVDS outputs should be observed, then the former resistors should be removed, and only R6 should be assembled.

PTN1111 is the other PTN product that could be evaluated absolutely independently, while PTN2111 and PTN3311 do require

some loop involvement. PTN1111's input signal could be either from the SMAs J6 and J8 or from PTN3322, as mentioned above. Where as the PTN 2111 could have its input signal from PTN1111–PTN3311 path or from PTN3322.

Two of the PTN1111 outputs– !Q9 & Q9 and !Q7 & Q7, and two of the PTN2111 outputs– !Q8 & Q8 and !Q6 & Q6, are connected to SMAs, and they allow for any type of measurements on the clock devices, including skew between outputs.

The input signal of PTN3311 must be provided by PTN1111. For the PTN3311 to be evaluated, resistors R27 and R28 should be soldered, and R23 and R24 should be dismantled. If simultaneous evaluation between PTN3311 and PTN2111 should be necessary, then PTN2111 must have its input from PTN3322. Please note that if all of the following four resistors R23, R24, R27, and R28 are on the board at the same time, there is just going to be double termination, so the quality of the signal might not be as desired and maximum performance is not guaranteed.

When the board is in the main mode of operation, PTN1111's and PTN2111's additional outputs could still be observed, and they will not affect the performance of the parts at all.

In the following appendix, attached are:

- Bill of materials
- Schematic
- Top layer layout and silk screen

SUPPORT

For further information, please, check www.philipslogic.com/networking or e–mail to PTN-Support@philips.com

To inquire about the availability of this board, please visit <http://www.philipslogic.com/products/ptn/evalboards/rqstptn>

To learn about other PTN boards, please visit <http://www.philipslogic.com/products/ptn/evalboards>

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APPENDIX

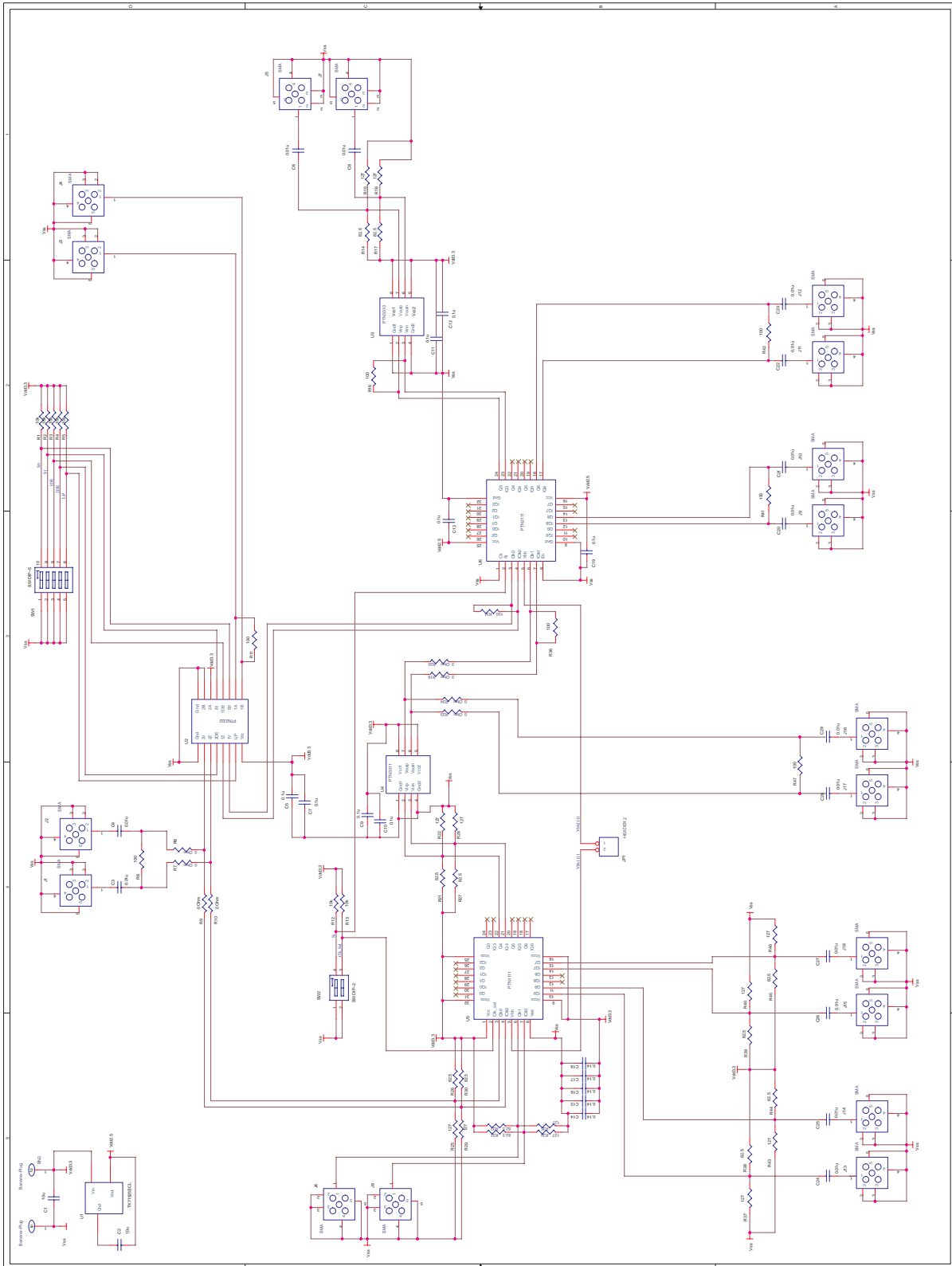
Bill of Materials

Item	Quantity	Reference	Part
1	2	BN2,BN1	Banana-Plug
2	2	C2,C1	Capacitor, 10 μ F
3	18	C3,C4,C5,C6,C8,C10,C11, C14,C24,C25,C26,C27,C28,C29,C30,C31,C32,C33	Capacitor, 0.01 μ F
4	13	C7,C9,C12,C13,C15,C16,C17, C18,C19,C20,C21,C22, C23	Capacitor, 0.1 μ F
5	1	JP1	Header 2
6	18	J1,J2,J3,J4,J5,J6,J7,J8, J9, J10,J11,J12,J13,J14, J15,J16,J17,J18	SMA Connector
7	7	R1,R2,R3,R4,R5,R16,R17	Resistor, 10 k Ω
8	8	R6,R15,R20,R35,R40,R45, R46,R51	Resistor, 100 Ω
9	14	R7,R9,R18,R21,R25,R30, R31,R34,R36,R37,R42,R43, R48,R49	Resistor, 82.5 Ω
10	14	R8,R10,R19,R22,R26,R29, R32,R33,R38,R39,R41,R44, R47,R50	Resistor, 127 Ω
11	8	R11,R12,R13,R14,R23,R24, R27, R28	Resistor, 0 Ω
12	1	SW1	DIP Switch-5
13	1	SW2	DIP Switch-2
14	1	U1,TK71525SCL	Voltage Regulator
15	1	U2, PTN3322	Universal Translator
16	1	U3, PTN3310	LVDS-PECL Translator
17	1	U4, PTN3311	PECL-LVDS Translator
18	1	U5, PTN1111	1:10 PECL Clock Distribution Device
19	1	U6, PTN2111	1:10 LVDS Clock Distribution Device

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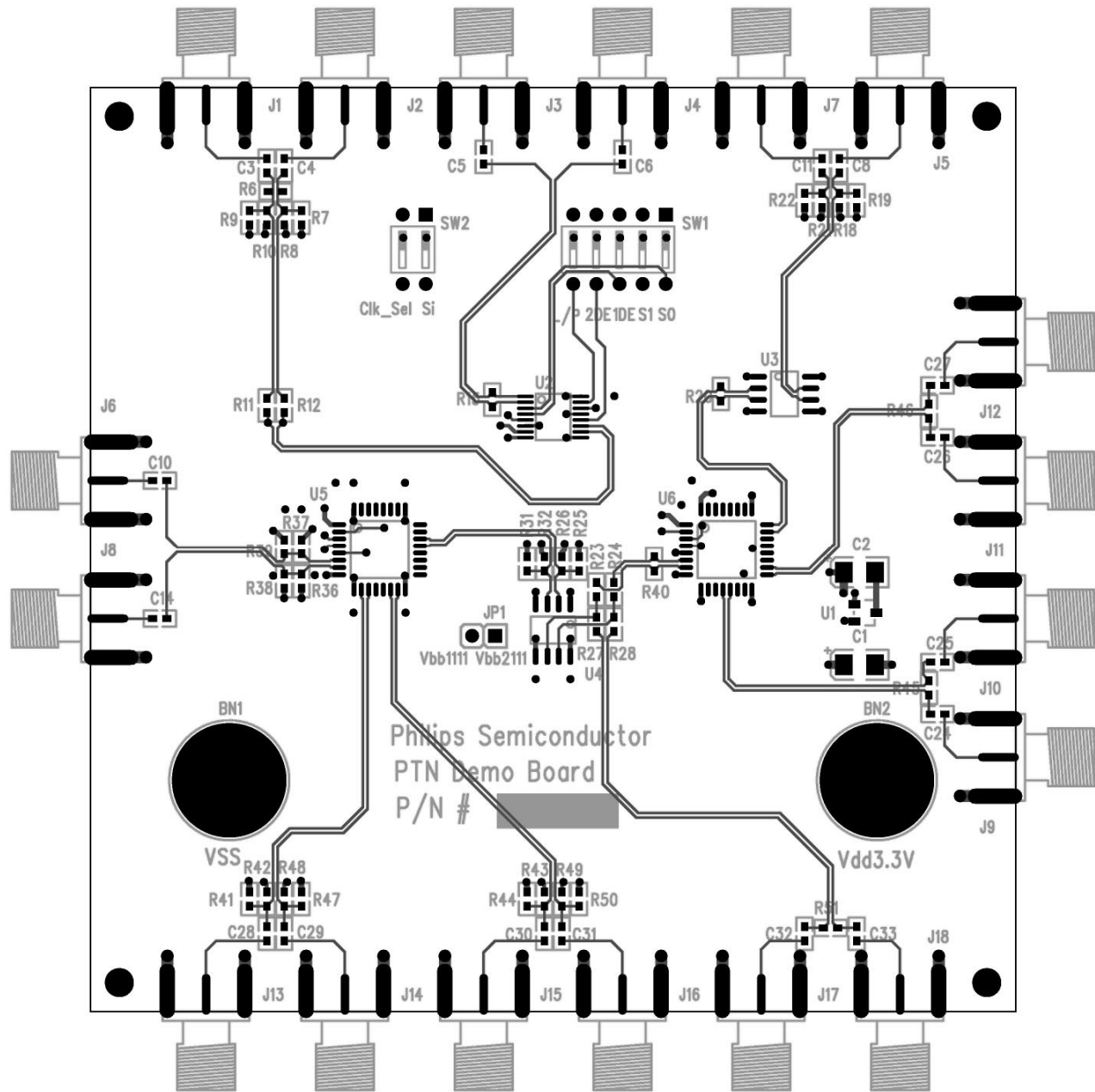
Schematic



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Top Layer Layout and Silk Screen



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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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