

# APPLICATION NOTE

## **AN253**

PTN3310 and PTN3311 LVDS-PECL translators  
bring significant benefits in high-speed networking  
and telecom applications

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AN253

## INTRODUCTION

Over the past years, dramatic changes and innovations have continued to take place in the technological world. New standards are introduced frequently, and in turn, they give birth to new logic families, I/O structures, voltage levels, and technology requirements, all of which offer their unique set of advantages and disadvantages. For the sake of simplicity, system architects and designers try to complete as much of their systems as possible using only one particular logic family and make their selection based on flexibility, speed of operation, noise immunity and cost. But, what works for one design does not always work for another. Often, the final result is the designer having to make choices of system components from many different vendors, with unmatched or conflicting interface requirements.

In the face of these difficulties, systems designers are often tempted to adopt new design strategies involving major commitment, investment, and change of methodology, in some cases even compromise their objective product performance. A design change in the ASIC of choice will only be justified by a promise of significant incremental revenue. Use of FPGAs often causes one to fall short of speed and performance goals. A change of supplier for a key system component involves risk and consumes time on a new learning curve.

Fortunately, system changes are not the only solution to system design challenges. In many cases, simple but high-performance interface solutions such as the Logic Translator can offer just the right amount of flexibility to solve the complex key component puzzle. In its basic form, the Logic Translator is a simple IC, which takes given signal level inputs (conforming to one standard) and produces different signal level outputs (conforming to another). The Logic Translator would ideally be so small, that it would not burden the already constrained board design and would be so perfectly functional that it would not be necessary for an already complicated ASIC to feature such logic internally.

With the introduction of PTN3310 and PTN3311, such unobtrusive Logic Translators exist. They have been developed under the Logic Product Group of Philips Semiconductors, targeted mainly for the telecom and networking infrastructure markets. In the telecom and networking world, two of the most popular standards for high-speed serial interconnects are PECL and LVDS, and the PTN3310/PTN3311 Logic Translators provide a simple way to mix and match system components based on either of these two technologies. PTN3310 provides translation from LVDS input to PECL output, and is complemented by the PECL to LVDS translation of the PTN3311.

For reference, brief overviews of these two popular high-speed signaling standards are given below.

## BASIC PROPERTIES OF LVDS

Low Voltage Differential Signaling (LVDS) allows for data transmission of several hundreds of Megabits per second. It is primarily used to interface between today's CMOS or BiCMOS ASICs supplied with 3.3V. As indicated in the name, LVDS is differential signaling. The complementary outputs have a small output swing, between 250mV and 400mV peak to peak, biased around a DC offset of 1.2V. Due to its differential mode of operation, the electromagnetic fields (ideally) tend to cancel, thus reducing electromagnetic interference and noise generation. With its low swing and current mode driver outputs, LVDS offers minimum

current spikes, low power consumption across frequency, and low noise. Figure 1 shows the basic LVDS voltage levels:

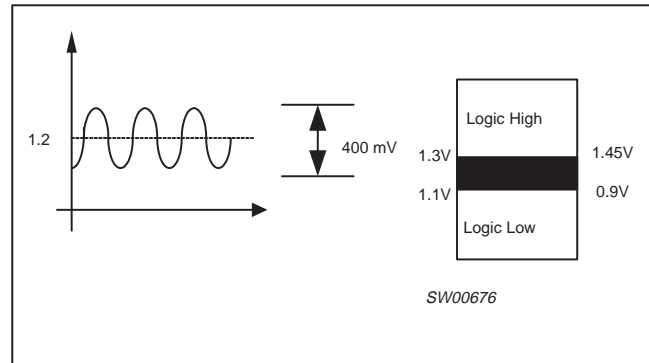


Figure 1. LVDS signal with switching levels

Regardless of the transmission medium – cable or PCB traces – the LVDS outputs must be terminated to the differential characteristic impedance in order to complete the current path and to terminate the high-speed signals properly. To prevent reflections and interference with other signals, LVDS requires a terminating resistor of 100 Ohms (that is, matched to the actual cable or trace) which should be placed across the differential signal lines, as close as possible to the receiver input. This simplicity of the LVDS termination makes it attractive and easy to implement in many applications. The following diagram shows the LVDS output definition:

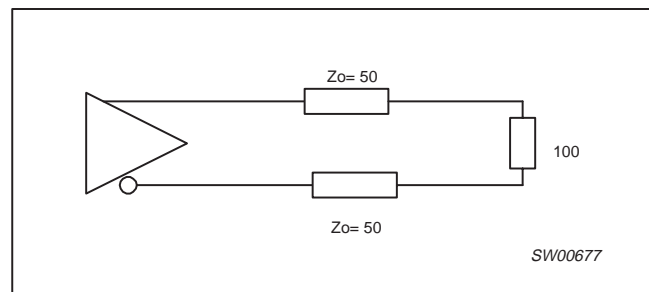


Figure 2. LVDS termination

To ensure reliability, the LVDS receiver has an internal fail-safe feature that forces the output to be in a known logic state (High) under certain fault conditions, such as floating, shorted and terminated inputs.

The major limitations of LVDS are its originally point-to-point nature and short transmission distance. For multi-drop applications and longer distances, LVDM and Bus-LVDS are largely similar alternatives.

## BASIC PROPERTIES OF PECL

Pseudo (or Positive) Emitter Coupled Logic (PECL) is in principle ECL referenced to a positive power supply. Its major advantage over ECL is that it doesn't have ECL's requirement of an additional power supply. Like LVDS, PECL is also based on differential signaling, but with a different offset and swing voltage. Typical V<sub>dd</sub> for PECL is 5V, but since today's advanced systems often favor a single 3.3V supply voltage, a new Low-Voltage PECL (LVPECL) standard has evolved.

# PTN3310 and PTN3311 LVDS-PECL translators bring significant benefits in high-speed networking and telecom applications

AN253

PECL is a low swing signal, and has a maximum swing of 800 mV. Both PECL and LVPECL are offset at  $V_{dd} - 1.32$ , where  $V_{dd}$  is 5 and 3.3 volts respectively. The diagram below shows the basic voltage levels for PECL:

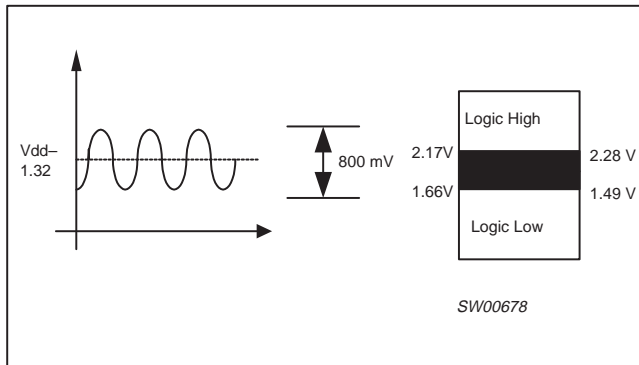


Figure 3. PECL signal with switching levels

The differential nature of the PECL circuit, with its differential amplifier input structure and complimentary outputs, makes it less vulnerable to induced common-mode noise, and makes it inherently ideal for differential applications. Also, the current drawn is constant during switching, so there are no supply current spikes. But probably one of the biggest advantages of PECL is its high-speed capabilities. Because of the fact that in ECL, transistors are not allowed to saturate, and because it basically makes use of a current-steering circuit (hence its name Current-Mode Logic or CML), very high speeds of operation are achievable. ECL is indeed the fastest of all logic families available today.

Unlike LVDS, though, PECL requires a more complex termination. PECL receivers commonly require pull down resistors to ground or termination resistor across the driver end, which in turn increases the amount of power dissipated. In general, there are various techniques for differential termination including standard, parallel, and Thevenin terminations, each approach having its application-specific benefits. The diagrams below show some of the most common termination techniques for PECL:

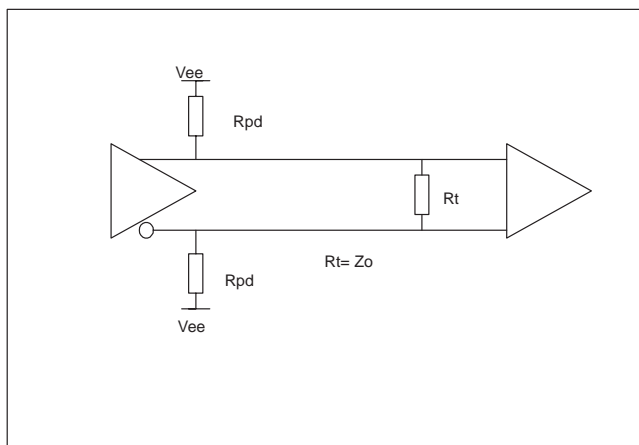


Figure 4. PECL Standard termination

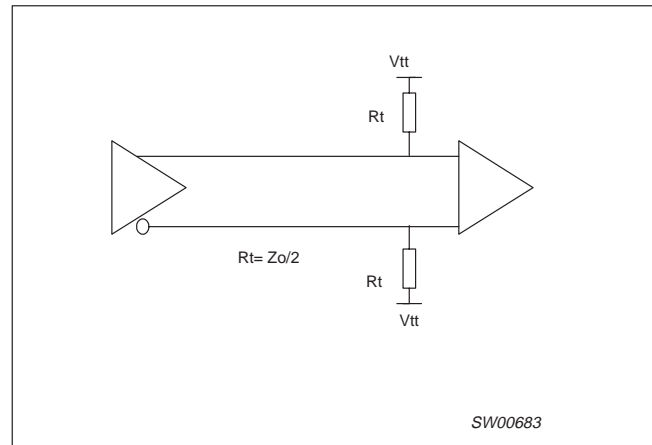


Figure 5. PECL Parallel termination

The major drawbacks of PECL are its power dissipation and the complexity of its termination.

### WHY THE LOGIC TRANSLATOR?

The Logic Translator offers some significant advantages over the common practice of using a combination of passive networks and active components to achieve the translation. In summary, it is a carefree "spot" solution, achieves perfect impedance and level matching simultaneously, does not require DC-free coding, and acts as a repeater by regenerating the signal.

In general, coupling or interfacing between PECL and LVDS I/Os can be achieved by using a network of capacitors and resistors. However, the additional devices will increase the overall power consumption and different coupling techniques must be applied between LVDS and PECL and PECL and LVDS. Adding additional components to the transmission medium and choosing their values must be done with care, in order to prevent any signal integrity issues. Picking the right value for the capacitance is of extreme importance and is closely related to the speed of operation. When choosing the value for a resistor, close attention must be paid in order to match the impedance of the medium in order to prevent any unwanted reflections, which can ultimately result in ringing. Both LVDS and PECL are sensitive to ringing due to their small signal levels. Moreover, reflections can cause interference with other signals, and in general improper termination can easily result in electromagnetic emission.

Interfacing between PECL and LVDS without additional components is possible, because the common mode range inputs of the PECL receivers are specified wide enough to process LVDS signals. However, the interface from LVDS to PECL is not so straightforward. Two DC levels must be provided before the signal enters the LVDS receiver, and the optimal resistor values needed for the proper signal levels are non-standard values in industrial (E) component value ranges. Moreover, the voltage swing at the LVDS receiver is decreased resulting in loss of noise margin. The following diagrams

# PTN3310 and PTN3311 LVDS-PECL translators bring significant benefits in high-speed networking and telecom applications

AN253

show a possible design interface between LVPECL and LVDS without the use of a Logic Translator:

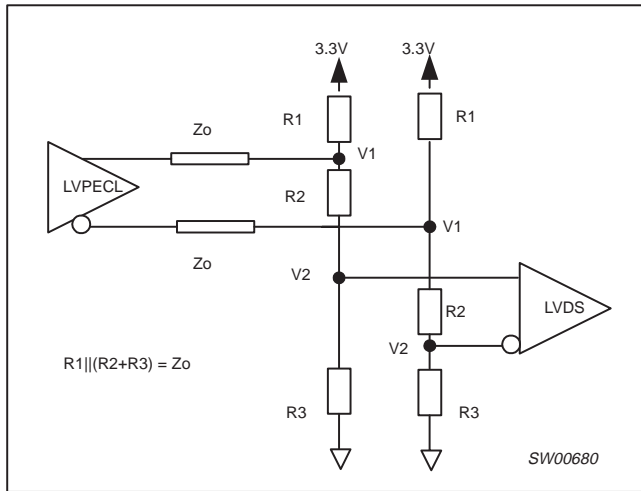


Figure 6.

For 50Ω controlled impedance line, the values for the termination resistors are as follows: R1= 83Ω, R2= 49Ω, R3= 76Ω.

For 100Ω controlled impedance line, R1= 253Ω, R2= 42Ω, R3= 124Ω.

Unterminated lines can be used only when the length of the interconnect is short (less than λ/4), and only parallel termination is required to match the impedance. However, this results in low impedance path due to the high output currents, which in turn results in increased power consumption.

Overall, the use of discrete components is a sophisticated solution requiring careful and repeated optimization, which can only limit, not enhance, the performance of the system.

By contrast, the Logic Translator is a care-free solution. When using the Logic Translator, the overall design of the board is simplified and no valuable engineering time needs to be spent determining resistor and capacitor values or on iterative design using board layout simulation. The difference in interfaces is taken care of by a small IC, which does not add much power consumption or propagation delay. It takes care of proper signal levels and signal integrity, and it does not take too much board space.

The PTN3310 and PTN3311 offer the optimal and the easiest solution for translating different-level signals. The system designer only needs to determine a suitable position for the compact package, and terminate the receivers or drivers properly, as required by the application. And that takes care of the signal incompatibilities that might exist. Moreover, the proper impedances are achieved, and the signal is regenerated, which is valuable if the signal must travel longer distance.

The proper termination schemes for PTN3310 and PTN3311 are shown on the diagram below:

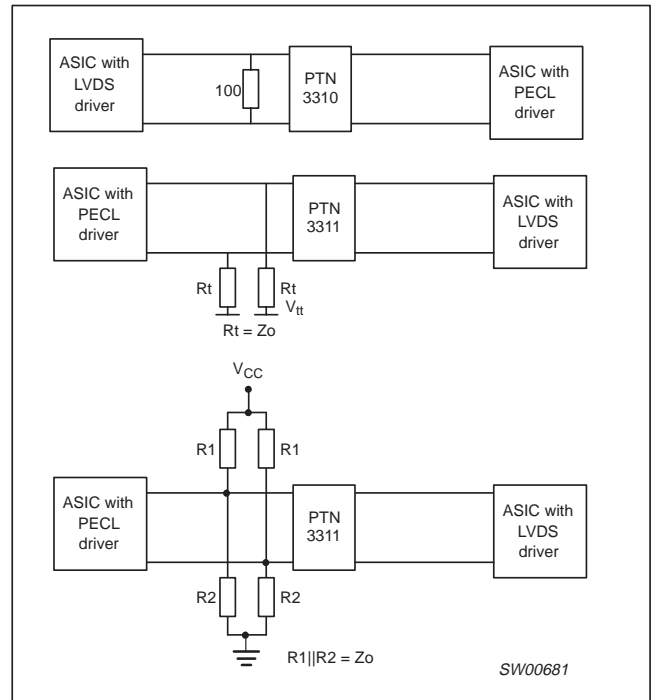


Figure 7.

The LVDS receiver requires 100Ω termination across the inputs. The PECL receiver requires 50Ω pull-down resistors. The termination resistors should be placed as close to the receiver as possible

# PTN3310 and PTN3311 LVDS-PECL translators bring significant benefits in high-speed networking and telecom applications

## AN253

### THE BIG PICTURE

Some examples for application of the high-speed, low-voltage LVDS and PECL in the Telecom and Datacom worlds are in switches, routers, hubs, add/drop multiplexers, network processors – point-to-point, box-to-box, rack-to-rack, etc.

As networks have become more powerful, their complexity has also increased. Electrons are coming out of the backplane's optical

transceivers with one signal level and need to propagate down the mother board with a different level; or are coming from one daughter card and need to go to another. The high-speed Logic Translators allow for the easy mixing right on the spot because they could be placed near the devices requiring the mixture of LVDS and PECL inputs and outputs. The following diagram shows a possible application of the high-speed serial Logic Translator:

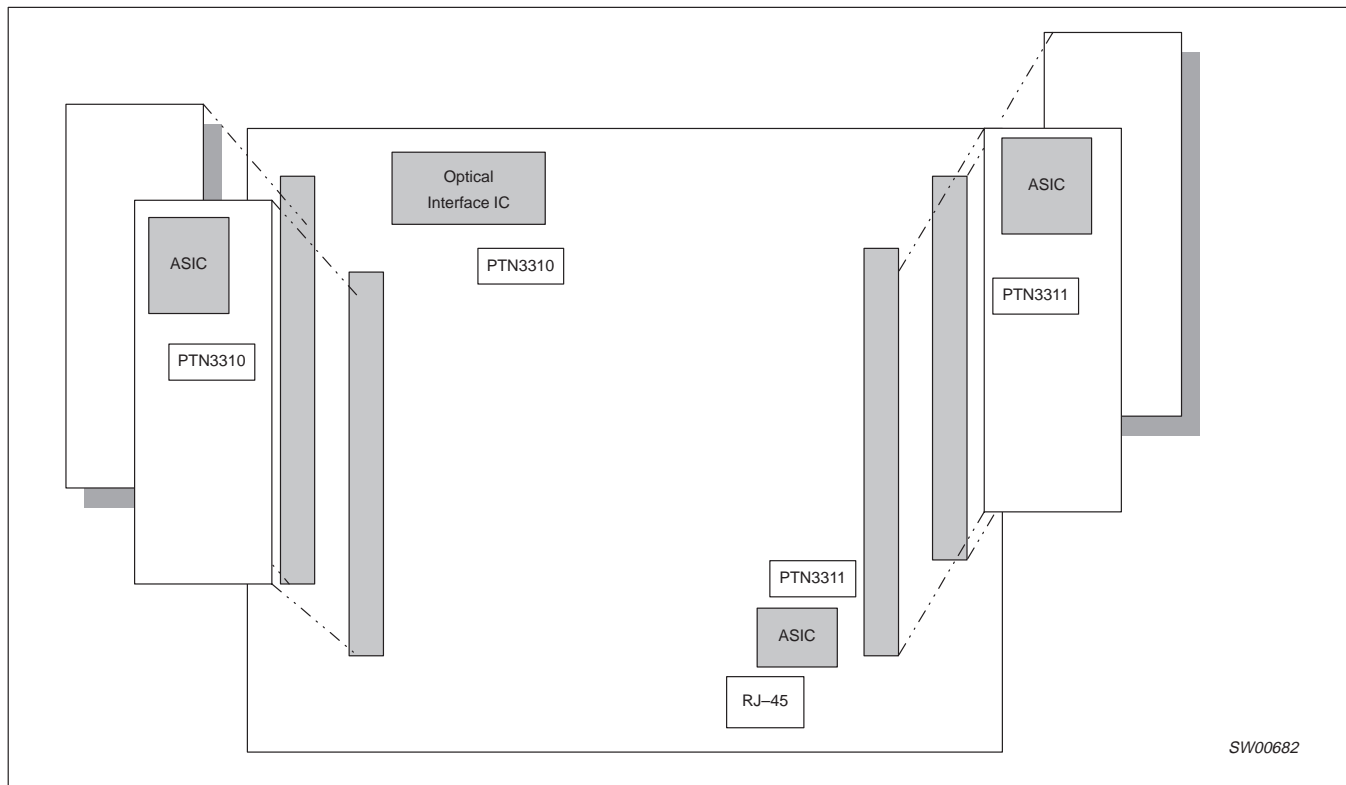


Figure 8.

Aside from the Networking world, the Logic Translator can be used in the PC and computing markets, as well as in the consumer communication products. For example, in flat panel displays, digital copiers, multimedia peripheral links, set top boxes and game display & control devices.

### ACKNOWLEDGEMENTS

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AN253

## Definitions

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AN253

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