AN10366

HVQFN application information

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Document information

Info	Content
Keywords	HVQFN package, board mounting
Abstract	This application note provides guidelines for the board mounting of HVQFN packages.

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Revision history

Rev	Date	Description
2	20060112	• Section 4.4 “Component placement” on page 12: amended text of first paragraph • Section 6: added text and tables following Table 4 on page 18
1	20050509	Application note AN10366_1

Contact information

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1. Introduction

This document provides guidelines for board mounting of HVQFN packages. Printed-Circuit Board (PCB) design, board mounting recommendations and board level reliability results are described.

The HVQFN package exposed die pad must be soldered to a corresponding solder land on the board for enhanced thermal, as well as electrical ground, performance. Thermal vias in the board solder land will improve heat transfer away from the package.

The following items affect soldering quality:

- Solder land pattern on the board
- Solder paste coverage and layout for terminals and exposed pad
- Type of solder paste
- Thermal vias
- Board thickness and structure
- Surface finish on the solder lands
- Finish of the terminal pads
- Reflow temperature profile

All of the above items need to be optimized for a high yield. The solder land dimensions, for example, are based on the package dimensions, but also on paste printing and component placement accuracy. It is also possible that the solder paste pattern for the exposed die pad may enter the region between the exposed pad and the lands, causing a bridge while the solder joint is good.

The guidelines given in this application note are based on extensive board mounting experiments with HVQFN packages with terminals having a pitch of 0.5 mm and 0.65 mm. Optimization trail, verification runs and reliability tests were carried out; however it should be emphasized that this is just a guideline to help the user in developing the proper board design and mounting process. Additional studies and development effort maybe needed to optimize the process for specific user surface mount practices and requirements.

This guideline can also be used for HVQFN terminals having smaller pitches than 0.5 mm.

2. Package introduction

2.1 Package description

The HVQFN is a near Chips Scale Package (CSP) Land Grid Array (LGA) type plastic encapsulated package with a copper lead frame base. The package has no leads or bumps, but an exposed pad in the center and peripheral land terminals at the bottom of the package. The terminals, together with the exposed pad, are soldered to the solder lands on the PCB, after solder paste is deposited.

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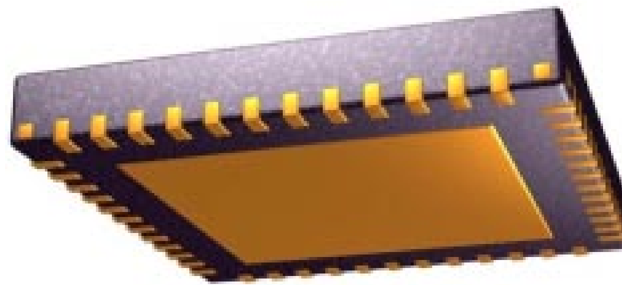

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Fig 1. HVQFN package (bottom view)

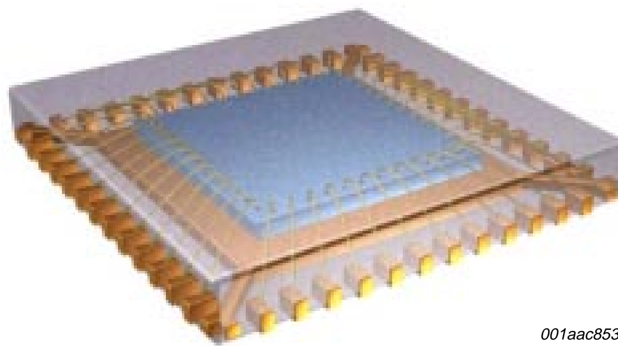

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Fig 2. HVQFN package (inside view)

The HVQFN package is currently available in a wide range of body sizes (i.e. 2.5 mm × 2.5 mm up to 12 mm × 12 mm) and terminal counts from 14 up to 100.

2.2 Outline versions

The HVQFN package is available in two different outlines. A map-molded sawn version and a single-molded punch-singulated version as depicted in Figure 3 and Figure 4.

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Fig 3. Sawn singulated version

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Fig 4. Punched singulated version

The HVQFN package shown in Figure 1, Figure 3 and Figure 4 is of the Full Connecting Bar (FCB) type. For this package it is possible to produce a solder fillet up the side of the component if the exposed bare copper is properly wetted. This may not be the case if the copper has oxidized during storage.

The other HVQFN type, with a Half-Etched Connecting Bar (HECB) is depicted in Figure 5. With this package type it is highly unlikely that a solder fillet will be formed due to the non-wettable package moulding compound.

Fig 5. Bottom view of a HECB type HVQFN package

The terminal finishes that are currently applied are pre-plated NiPdAu, post-plated PbSn, or post-plated matte Sn.

The reflow soldering process settings described in this application note are based on an experimental study using the following packages:

- HVQFN with a body size of 7 mm × 7 mm and a pitch of 0.5 mm; its exposed die pad is 5.1 mm × 5.1 mm
- HVQFN with a body size of 4 mm × 4 mm and a pitch of 0.65 mm; its exposed die pad is 2.1 mm × 2.1 mm

All these packages are of the FCB type with NiPdAu pre-plated terminals.

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3. Printed-circuit board lay out

3.1 Solder lands, mask layout

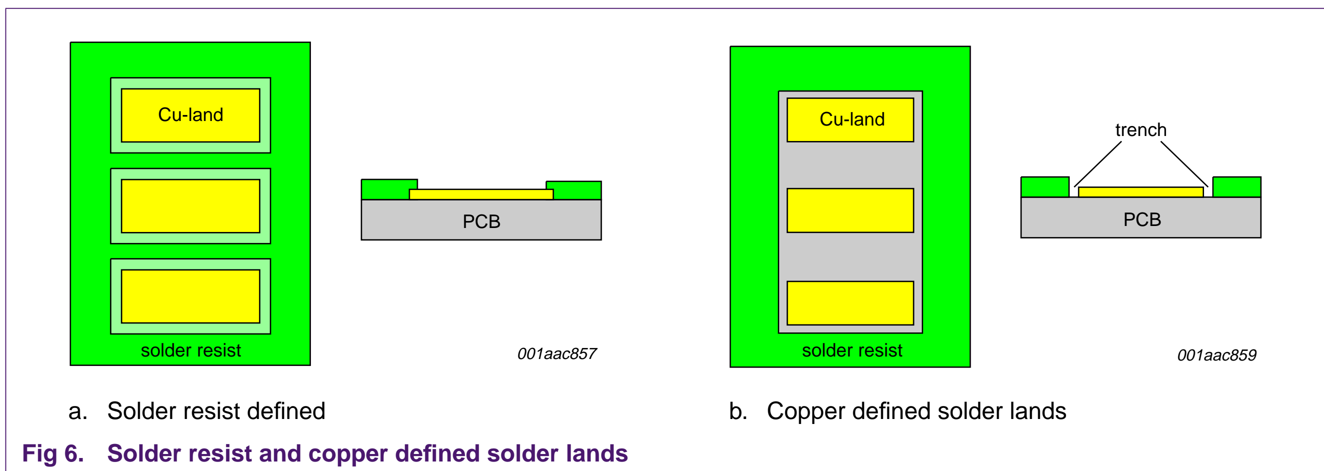
Typically, the solder lands on the Printed-Circuit Board (PCB) are made of Cu. A solder resist layer is applied around the solder pads in order to limit the solder flow on the solder lands. In such cases the soldering area is Solder Resist Defined (SRD) or Solder Mask Defined (SMD). Because SMD has several meanings, the term SRD is used instead.

Depending on the terminal pitch of the device (≤ 0.5 mm) and/or the available PCB technology, the spacing between the terminals may not allow the application of solder resist. In that particular case the solder land is Non Solder Resist Defined (NSRD).

A combination of SRD and NSRD may occur when, for example, the spacing between the solder land of the terminal and the solder land of the exposed pad is large enough. In this case NSRD can be applied between terminal solder lands, and SRD can be applied between exposed pad terminal lands.

3.1.1 Solder land layout

The copper must extend 50 µm below the solder resist on all sides of the solder land. In Figure 6a, yellow is copper and dark green is solder resist. The yellow/green border is copper below the solder resist.



a. Solder resist defined

b. Copper defined solder lands

Fig 6. Solder resist and copper defined solder lands

For HVQFN packages with a pitch of 0.5 mm or less, the distance between two solder lands is too narrow for them to be solder resist defined. Therefore, the solder lands for the HVQFN are Cu defined as shown in Figure 6b.

In Figure 7, grey is the bare board and light green is the copper solder land below the solder resist. Therefore, the solder land short sides are solder resist defined, but their long sides are copper defined.

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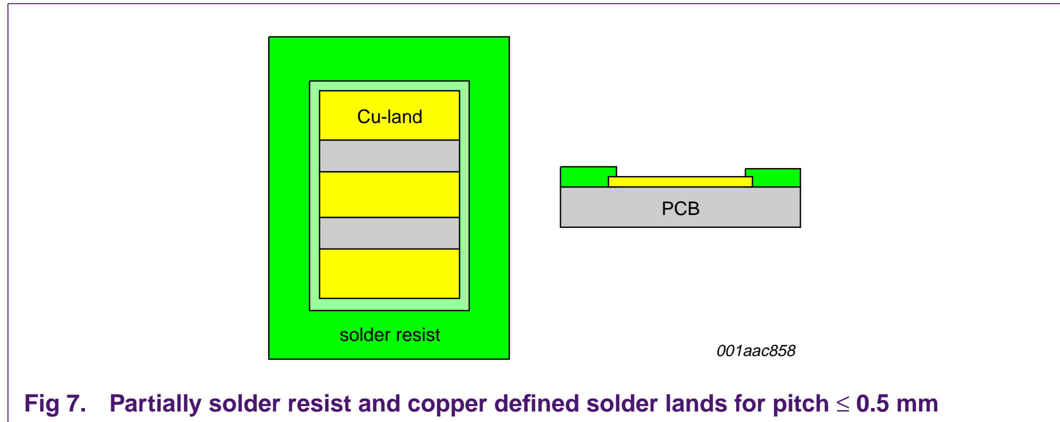
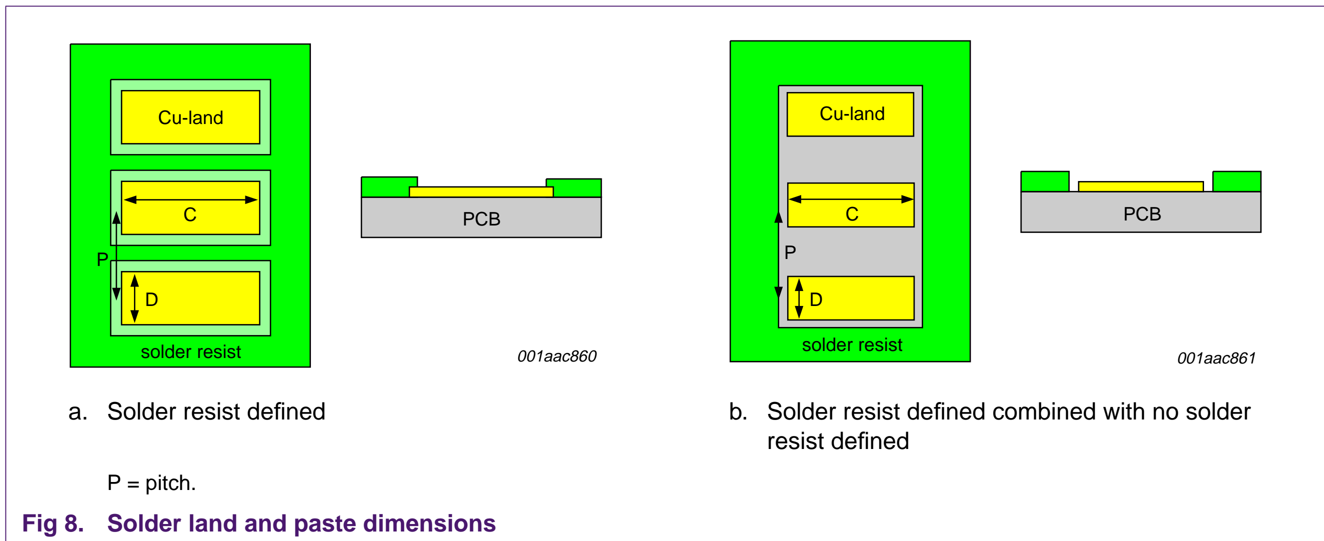


Fig 7. Partially solder resist and copper defined solder lands for pitch ≤ 0.5 mm

The solder land dimensions are defined in Figure 8.



a. Solder resist defined

b. Solder resist defined combined with no solder resist defined

P = pitch.

Fig 8. Solder land and paste dimensions

The solder land dimensions for the HVQFN with 0.5 mm and 0.65 mm pitch board layouts are summarized in Table 1. Dimensions C and D represent the length and width of copper of the solder land. The solder resist and stencil aperture dimensions are derived from dimensions C and D.

Table 1: Pitch and solder land dimensions (mm)

Pitch	C	D
0.5	0.90	0.29
0.65	1.10	0.30

The values listed in Table 1 were obtained from a program specifically developed for reflow soldering of components having a high degree of miniaturization, and are based on extensive practical experience.

As solder joint formation relies entirely on solder paste applied by stencil printing, it is imperative that solder paste is applied correctly. Solder paste deposits must be placed 25 μm away from the edge of the solder land at all sides i.e. a stencil aperture dimension is 0.05 mm smaller than the solder land dimensions (C and D). Thereby preventing solder paste bridge formation when paste bulges during component placement.

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Note that the solder lands extend beyond the edges of the package, thereby increasing the occupied area on the board. This is necessary, for proper solder paste printing. If the solder land dimensions are equal to those of the component leads, the stencil apertures will become too small for proper solder paste release; paste will tend to adhere to the stencil apertures resulting in either incomplete or no solder joint between solder land and package terminal. Furthermore, extending the solder land beyond the component edge will increase the probability of fillet forming.

The same board may be used for both FCB and HECB type HVQFN packages.

In case of the HECB type, the small section of non-wetting package will be placed over the solder paste.

The solder lands may not be too wide, as this would increase the risk of bridging to adjacent solder lands.

3.1.2 Exposed pad solder lands

For optimal heat transfer, the exposed die pad needs to be soldered to a large solder land. However for the larger packages, with a large exposed pad, eliminating voids is almost impossible. Voids are formed when the solder paste melts and the distance to the edge of the solder land is too far. The voids remain trapped between the component and the board. Gas from uncapped thermal vias may also add voids.

The perimeter of the exposed pad solder land should be solder resist defined.

During reflow soldering, solder paste melts and gas or trapped air is released, causing splattering or solder balling. Solder balling and splatter are minimized if the solder paste is printed as a number of individual dots, instead of one large deposit, and if the solder paste is kept at a sufficient distance from the edge of the solder land.

The solder paste pattern area should cover 35 % of the solder land area. When printing solder paste on the exposed die pad solder land, the solder paste dot area should cover no more than 20 % of this solder land area. Furthermore, the paste should be printed away from the solder land edges. This is illustrated in Figure 9; the solder paste pattern area lies within the boundary indicated by the red line and it is divided by the entire solder land area.

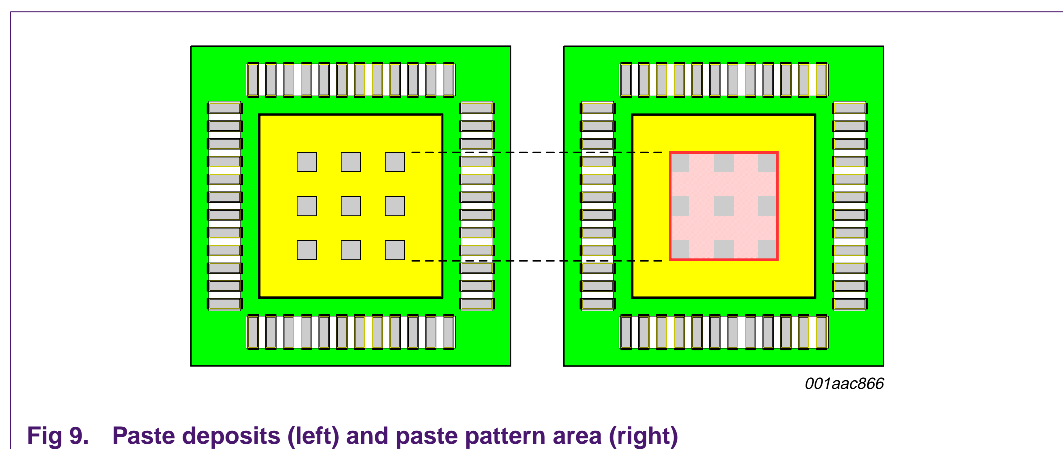

Fig 9. Paste deposits (left) and paste pattern area (right)

Using the definitions of Figure 9, the solder paste dimensions for HVQFN with 0.5 mm pitch and for HVQFN with 0.65 mm pitch are given in Table 2.

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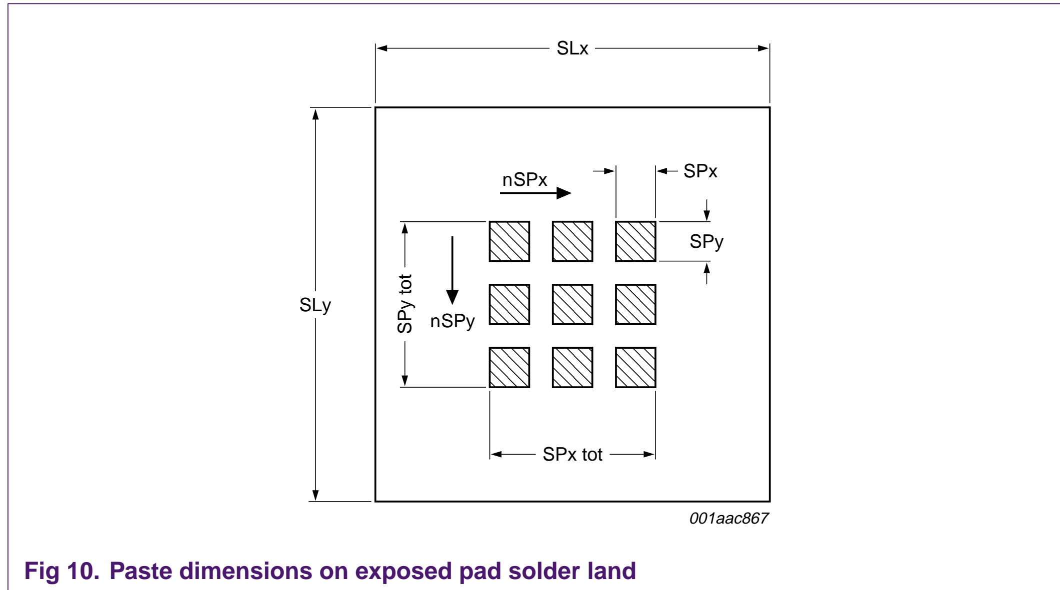

Fig 10. Paste dimensions on exposed pad solder land

Note: Sometimes it is not necessary to solder the exposed die pad to the board. In that case the solder paste can be omitted.

Table 2: Solder paste dimensions on exposed pad solder land (mm)

P	Body	SLx	SLy	nSPx	nSPy	SPx tot	SPy tot	SPx	SPy
0.5	7 × 7	5.10	5.10	3	3	3.00	3.00	0.75	0.75
0.65	4 × 4	2.00	2.00	2	2	1.20	1.20	0.45	0.45

Thermal vias must be incorporated in the exposed pad solder land to transfer heat away from the package to the board. If possible, these thermal vias should be capped with copper in order to reduce the impact on the soldering process. Other options are filling the vias with epoxy (heat transfer will be provided by the copper via walls), or allowing solder resist to encroach the bottom of the via. If the bottom of the vias are encroached, care must be taken to prevent air being trapped inside the via which may cause defects during the reflow solder process. When vias are not completely filled, more solder paste has to be printed on the exposed pad solder land to fill the cavity.

The number of thermal vias that must be incorporated in the exposed pad solder land will have to be determined for each individual application. Because of the above mentioned risk of solder absorption by incompletely filled vias, it is best if no more vias than necessary are used. In addition, the pattern of thermal vias should be designed so that solder paste is not printed on top of the vias. This way, the solder will be less likely to run into the vias, and air will not be trapped in the vias.

Experiments were performed with a 4-layer FR4 board with a NiAu finish.

3.2 Generic footprint

The board mounting investigation was done using a small and a medium sized package i.e. the HVQFN with 4 mm × 4 mm body and the HVQFN with 7 mm × 7 mm body.

Since the introduction of HVQFN packages the number of lead counts, body sizes and exposed pad dimensions has grown rapidly.

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Figure 11 and 12 provide clear and comprehensive footprint information for board mounting an HVQFN package. The generic footprint pattern shown in Figure 11 only shows the dimension variables; actual dimension values of a specific package type are tabulated below its footprint diagram.

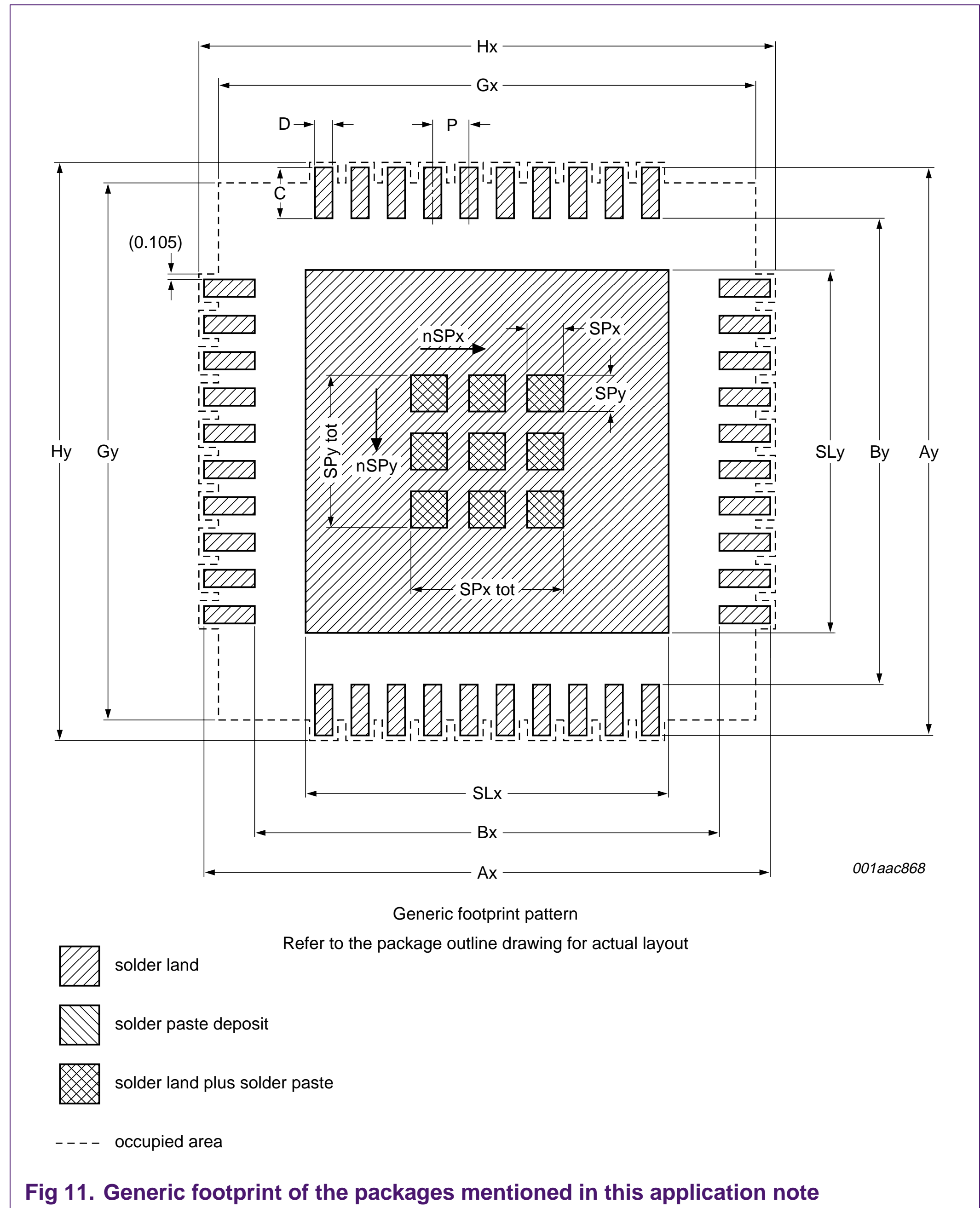

Fig 11. Generic footprint of the packages mentioned in this application note

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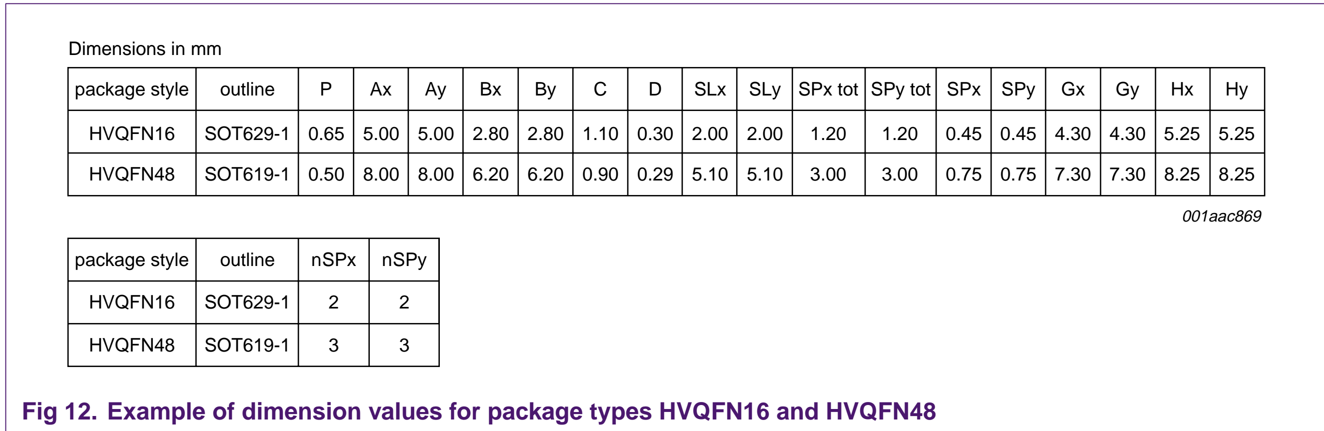

Dimensions in mm

package style	outline	P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
HVQFN16	SOT629-1	0.65	5.00	5.00	2.80	2.80	1.10	0.30	2.00	2.00	1.20	1.20	0.45	0.45	4.30	4.30	5.25	5.25
HVQFN48	SOT619-1	0.50	8.00	8.00	6.20	6.20	0.90	0.29	5.10	5.10	3.00	3.00	0.75	0.75	7.30	7.30	8.25	8.25

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package style	outline	nSPx	nSPy
HVQFN16	SOT629-1	2	2
HVQFN48	SOT619-1	3	3

Fig 12. Example of dimension values for package types HVQFN16 and HVQFN48

Footprint information for reflow soldering of specific HVQFN packages is available under ‘Package information’ on the ‘Product information’ page of the Philips Semiconductors web site at the URL given in “Contact information” at the bottom of page 2. The unique identifier for the footprint is the Philips package version (the package SOT number).

4. Board mounting recommendations

4.1 Solder paste

The following solder pastes were used in the evaluation and gave satisfactory results:

- PbSn paste: Alpha Metals Omnix 5002 (62 % Sn, 36 % Pb, 2 % Ag)
- SAC paste: Alpha Metals Omnix 310 (95.5 % Sn, 4 % Ag, 0.5 % Cu)

Both of these solder pastes are ‘no-clean’; due to the small stand-off height of the HVQFN, proper cleaning underneath the package is not possible.

4.2 Stencil

An electroformed stencil of 125 μm thickness is recommended for HVQFN with a terminal pitch of between 0.5 mm to 0.65 mm. For a HVQFN with a pitch larger than 0.65 mm, a 150 μm stencil may be used, and for a pitch smaller than 0.5 mm, a 100 μm stencil is recommended.

4.3 Solder paste and deposit inspection

Solder paste deposits should be inspected according to Figure 13 and should correspond at least to class 3. If they do not reach the required height, and are classified as ‘2’ or less, the paste is not properly released from the stencil aperture, and the stencil should be cleaned.

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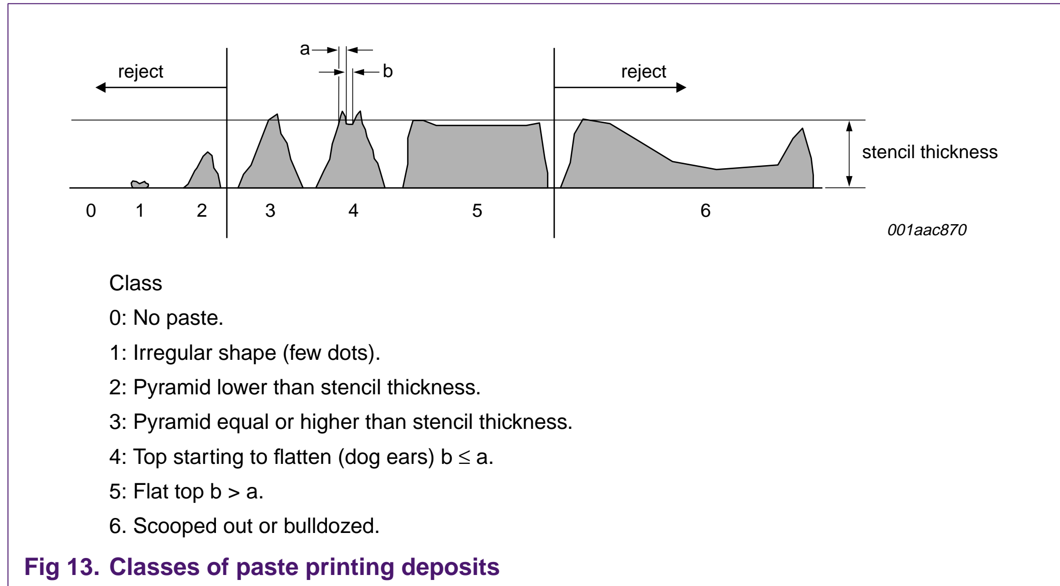

Class

0: No paste.

1: Irregular shape (few dots).

2: Pyramid lower than stencil thickness.

3: Pyramid equal or higher than stencil thickness.

4: Top starting to flatten (dog ears) b ≤ a.

5: Flat top b > a.

6. Scooped out or bulldozed.

Fig 13. Classes of paste printing deposits

Paste smearing should be classified according to Figure 14. Smearing below class 3 is no longer acceptable and the stencil must be cleaned. In this case, it is also important to clean the bottom of the stencil (the board side), as solder paste may have accumulated there.

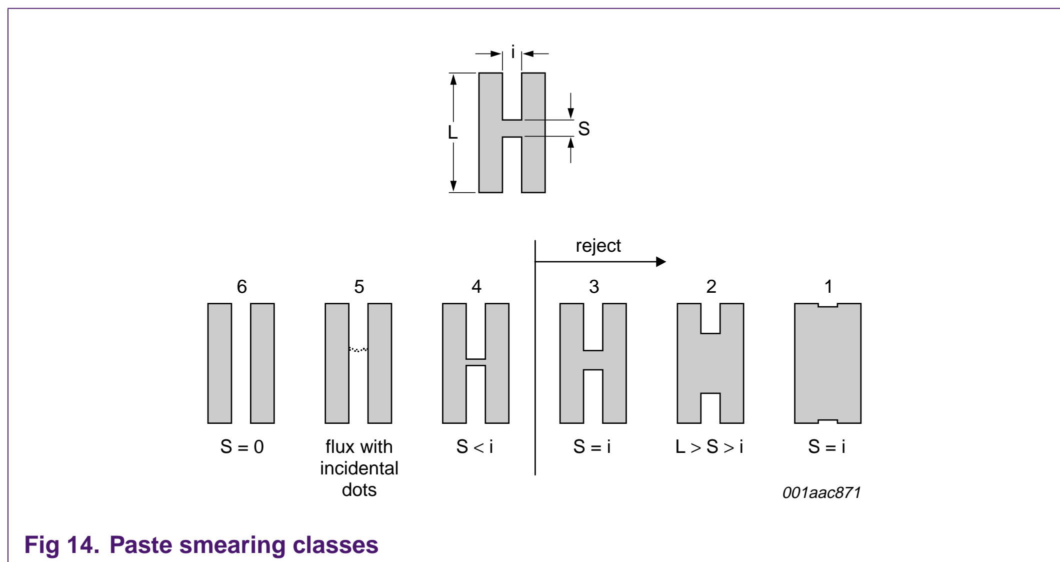

Fig 14. Paste smearing classes

4.4 Component placement

Depending on their moisture sensitivity level, HVQFN components are dry packed. If packages are removed from their sealed dry bags and not soldered within their out-of-bag time, they must be dry baked at 125 °C for 4.5 hours prior to placement and reflow. After dry bake, packages can be either stored in dry Nitrogen or resealed in appropriate dry bags.

The components should be placed with a placement machine, preferably with a placement accuracy better then 50 µm.

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4.5 Reflow soldering and conditions

When reflow soldering, it is imperative that each and every solder joint reaches a peak temperature that is:

- High enough so that a proper joint is made (this depends on the solder alloy); this is the minimum peak temperature,
- Low enough that the components and boards are not damaged; this is the maximum peak temperature

As a result, there is a range of temperatures that lie between the minimum and maximum peak temperatures that forms the process window in which proper solder joints will be made.

In reflow soldering, HVQFN components on a board will reach higher temperatures than large components. Yet, all components' peak temperatures must lie within the range of peak temperatures that results in a good solder joint. Therefore, oven temperature settings, conveyor belt speeds, and even board layouts must be optimized so that this is attained.

For PbSn solder a minimum temperature of 205 °C is required to form reliable joints. For SAC solder this temperature is 235 °C.

When a lead-free solder is substituted for a PbSn solder, the range of allowed peak temperatures is reduced. The maximum allowable peak temperature is not changed (boards and components are still damaged beyond a certain temperature). However, most lead-free solders have a higher melting temperature than PbSn solders, so that the minimum allowable peak temperature is higher. As a result, all components have to be squeezed into a peak temperature range that is narrower than when PbSn is used, which requires a tighter process control.

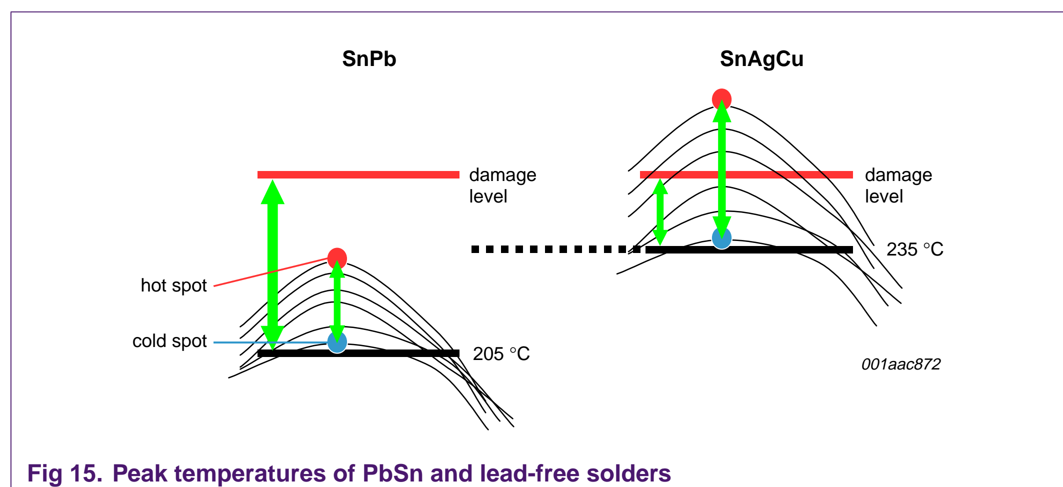

Fig 15. Peak temperatures of PbSn and lead-free solders

HVQFN packages may be reflow soldered according to the common process flow shown in Figure 16.

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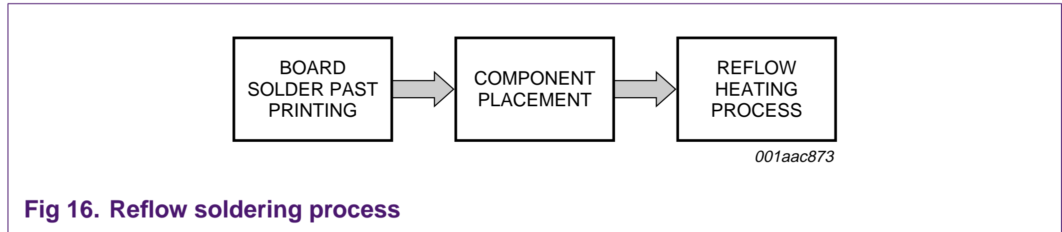

Fig 16. Reflow soldering process

A convection oven should be used for reflow soldering. The reflow soldering profile according to J-STD-020C is shown in Figure 17.

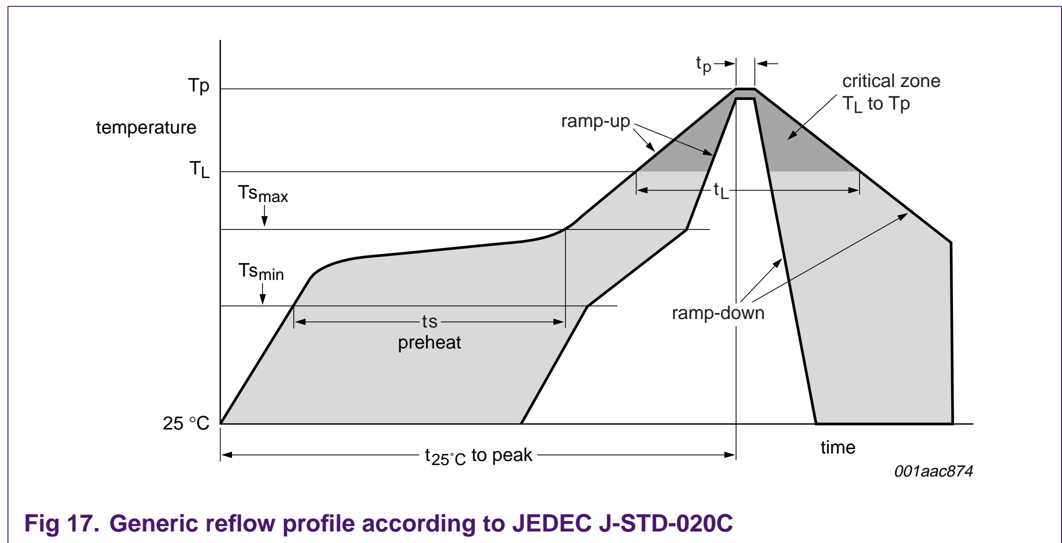

Fig 17. Generic reflow profile according to JEDEC J-STD-020C

3 zones can be distinguished i.e. preheat, ramp-up to soldering temperature and ramp down to ambient. The profile description is derived from J-STD-020C and is shown in Table 3.

Table 3: Reflow profile description according to J-STD-020C

Reflow condition	SnPb process	Pb-free process
Lower package temperature	205 °C	235 °C
Maximum package temperature	(240 + 0/–5) °C	(260 + 5/–0) °C

The profiles for PbSn and lead-free pastes as used for this evaluation are shown in Figure 18 and Figure 19. These profiles match the recommendations from the solder paste supplier. A Nitrogen atmosphere is not necessary.

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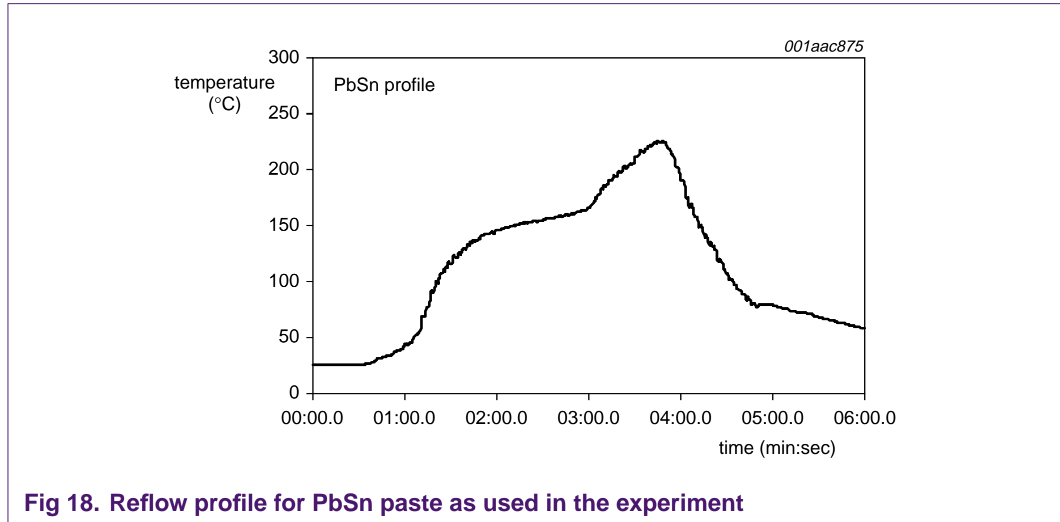

Fig 18. Reflow profile for PbSn paste as used in the experiment

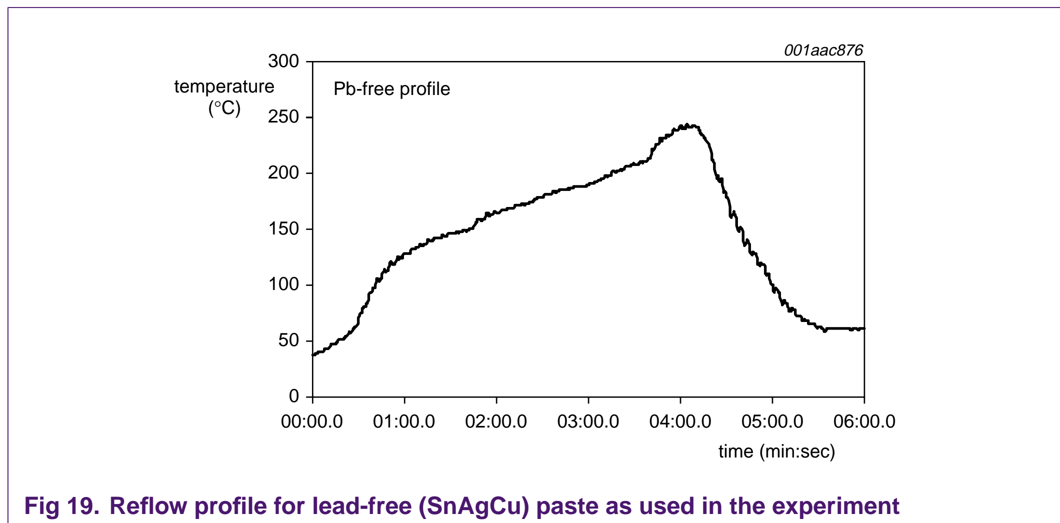

Fig 19. Reflow profile for lead-free (SnAgCu) paste as used in the experiment

HVQFN solder joints can be checked by X-ray. Short circuits, and large solder balls are easily detected. An X-ray photograph of a soldered HVQFN is shown in Figure 20.

Note: Small solder balls - solder balls that are smaller than one-third of the distance between two solder lands - are considered harmless. Solder balls larger than half the distance between two solder lands should be avoided. Such solder balls will be embedded in the flux underneath the component, and are not likely to cause any damage but give the impression that the paste printing process is not optimized.

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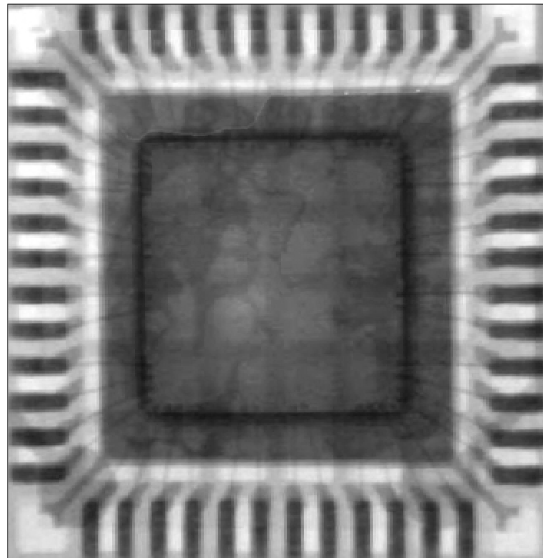

Fig 20. X-ray photograph of soldered HVQFN

Figure 21 shows detail of a cross-section of a HVQFN solder joint. Note that the fillet does not reach the top of the bare copper side. However, the slant of the fillet, and the contact angle, imply that a good joint has been made. A fillet is not necessary for a joint, but it will improve the joint reliability. Fillet formation will depend on possible oxidation of the bare copper at the terminal sides.

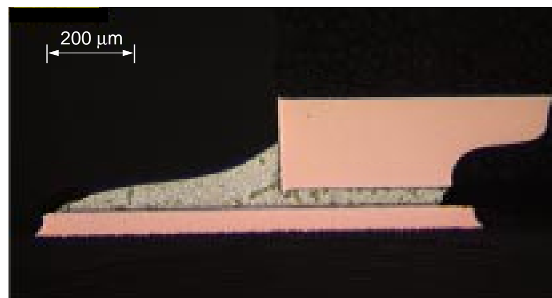

Fig 21. Cross-section of a HVQFN solder joint

5. Repair or rework instructions

When an HVQFN package on a board needs to be replaced, the following rework process flow should be applied:

1. Device removal.
2. Site preparation.
3. Solder paste printing.
4. Device placement.

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5. Reflow soldering.

Prior to the above mentioned process flow, the board should be dry baked for 4 hours at 125 °C.

5.1 Device removal

It is essential when removing an HVQFN package that the board is uniformly heated to avoid board warpage.

The topside of the device is heated with a hot air gun with a small orifice nozzle to a temperature that is close or equal to the actual reflow temperature. Depending on the chosen de-soldering technique the device can then be removed with a pair of tweezers or a vacuum nozzle.

5.2 Site preparation

After removal of the device the site must be prepared for the new device. Prepare the site by removing any excess solder and/or remaining flux. This can be done at a suitable de-soldering station, using a sucker, solder wick or other available technique.

Note: Apply a temperature that just melts the solder but not damage the board.

5.3 Solder paste printing

Apply solder paste to either the prepared site or the device. A miniature stencil or other suitable techniques can be used.

5.4 Device placement

The last steps of the repair process is to place and solder the new HVQFN package on the board. Align the HVQFN using a microscope or split beam system. If this is not possible, align the device with any board markers.

5.5 Reflow soldering

Apply a reflow soldering condition which is as close as possible to the board mounting recommendation (see Section 4.5).

6. Board level reliability assessment results

For this assessment, HVQFN packages with a body size of 7 mm × 7 mm and a pitch of 0.5 mm and HVQFN packages with a body size of 4 mm × 4 mm and a pitch of 0.65 mm have been mounted on a PCB. The reliability of the solder joint between the package terminals and the PCB solder lands (second level interconnect reliability) have been verified.

A daisy chain pattern between the board and the packages has been used to check solder joint degradation. The daisy chain pattern goes from the first package terminal via the Si-die to the second package terminal and is connected through the solder lands to the third package terminal. In this way terminals 1 to 2, 3 to 4, 5 to 6 etc. are internally

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connected and terminals 2 to 3, 4 to 5, 6 to 7 etc. are externally connected. By measuring the change in resistance between the first and the last terminal, a failed connection can be detected.

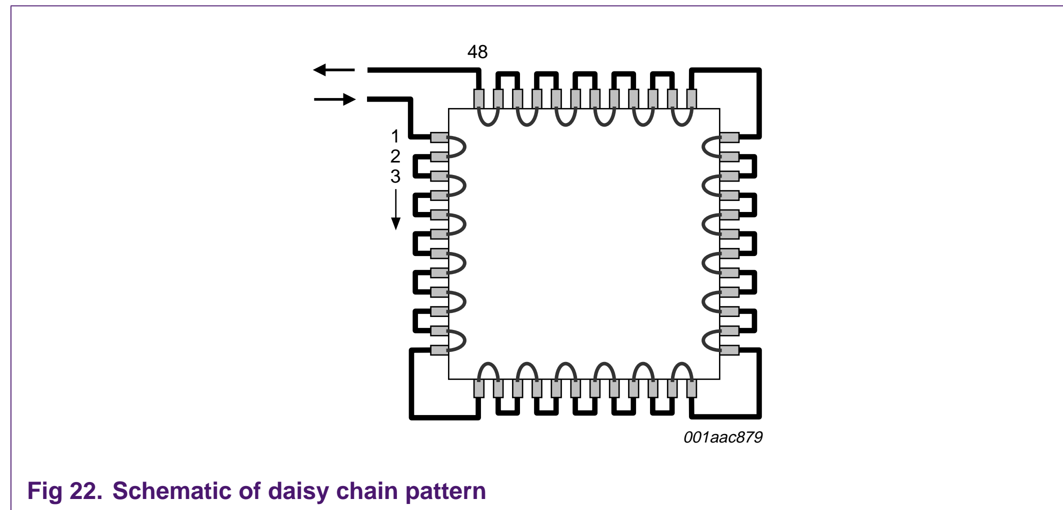

Fig 22. Schematic of daisy chain pattern

The HVQFN packages that have been mounted conform to this application note recommendation. Key characteristics of the PCB are listed in Table 4.

Table 4: PCB characteristics

Board parameter	Material or quantity
Board material	FR4
Board thickness	1.2 mm
Number of layers	4
Board finish	NiAu

Age accelerating test conditions were chosen which went beyond normal life conditions. The devices were shock tested in air-to-air Thermal Shock Test (TST), alternately exposed to a chamber kept at –40 °C and a chamber kept at +125 °C. Transition time between the two chambers was a few seconds. The dwell time at the extreme temperatures was 30 minutes, which resulted in a total cycle time of 1 hour. The test was performed according to IEC Standard 60068-2-14.

For each solder type, four boards were tested. Each board was fitted with 15 HVQFN48 packages and 45 HVQFN16 packages resulting in a total of 240 packages per solder type. At the end of the TST (2000 cycles), the HVQFN16 showed no failures for both the PbSn- and Pb-free solder. Therefore a log normal distribution could not be generated. For the larger HVQFN48 package, the number of cycles till failure are presented by a log normal distribution. The log normal distribution is described by two parameters, μ (the mean) and σ (the standard deviation). Test results for the two solder types of the HVQFN48 are listed in Table 5.

Table 5: Log normal distribution for HVQFN48 with PbSn- and Pb-free solder (TST)

Parameter	PbSn	Pb-free
Sample size	60	60
μ	7.6986	7.7212
σ	0.2033	0.3793

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On the basis of the log normal distribution and the number of temperature cycles, the number of solder joint failures can be calculated after which a certain percentage of devices fail. These results are summarized in Table 6.

Table 6: HVQFN48 solder joint defect rate versus number of temperature cycles (TST)

Defect rate	Temperature cycles	
	PbSn	Pb-free
0.1 %	1087	603
1 %	1246	777
10 %	1487	1081
50 %	1803	1550

For smaller package HVQFN16 it is expected that the MTBF is above 2500 cycles.

The TST described above was found to be too harsh for real application conditions, whereas the Temperature Cycling Test (TMCL) is a closer match to application conditions. Therefore, a subsequent TMCL was performed on the HVQFN48 having Pb-free solder. The characteristics of the PCB used are identical to those of the TST, see Table 4. The temperature swing and cycles per hour are also identical to those in the TST (–40/+125 °C and 1 cycle per hour). However, the ramp and dwell times are different, being 10 minutes and 20 minutes respectively. The test was performed on 64 packages for 3654 cycles, and the results are summarized in Table 7.

Table 7: HVQFN48 log normal distribution for TMCL with Pb-free solder

Parameter	Pb-free
Sample size	64
μ	8.2380
σ	0.2485

On the basis of the log normal distribution and the number of temperature cycles, the number of solder joint failures can be calculated after which a certain percentage of devices fail. These results are summarized in Table 8.

Table 8: HVQFN48 Pb-free solder joint defect rate versus number of temperature cycles (TMCL)

Defect rate	Pb-free temperature cycles
0.1 %	1755
1 %	2120
10 %	2750
50 %	3780

The following conclusions can be made based on the results of the TST and TMCL:

- MTBF is affected by the test conditions (TST or TMCL)
- TMCL results are factors 2 to 3 better than the TST results

The TMCL is found to be more representative of real application conditions, and the results of this test should be used for reference.

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Since HVQFN packages are mounted directly on the board, interactions with the board have a relatively large impact on joint reliability. The HVQFN package internal construction, board structure and board thickness can influence solder joint reliability. In order to reach a high level of solder joint reliability these factors should not be neglected.

Although the results described above are accurate, it is the assembler's responsibility to verify the board level reliability on a package-by-package basis for each board and assembly technology.

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7. References

[1] **J-STD-020C July 2004 —** Joint Industry Standard Moisture/Reflow, Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.

[2] **IEC standard 60068-2-14 —** Environmental testing.

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