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Ensure data integrity with real-time data error detection

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Document information

Info	Content
Keywords	real-time data error detection, data checking, UART advanced feature
Abstract	The Real-Time Data Error Detection technology is an enhanced feature to the Impact line of Philips Semiconductors industrial UARTs. The benefit of using the feature is for ensuring data integrity in long distance transmission and reception. The advantage of implementing the real-time data error detection is explained and the operation of the real-time error checking systems is described in this application note. This application note is applicable to the following Philips Semiconductors industrial UARTs: SC28L201 (1-channel) and SC28L202 (2-channel) UARTs.

PHILIPS

Revision history

Rev	Date	Description
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1. Introduction

Philips Semiconductors, the world's leading supplier of Universal Asynchronous Receiver Transmitter (UART) devices for industrial applications, developed the industry's first UART with Real-Time Data Error Detection feature to significantly reduce the amount of time required for performing bit-by-bit real-time error checking during data transmission. The real-time data error detection technology improves system data integrity performance by checking data for accuracy as it is being transmitted so the processor does not have to spend time on evaluating the data transmission upon return. In addition, the real-time data error detection technology generates an interrupt signal to notify the processor as soon as any errors are identified. Then, the microprocessor can read the information to determine the interrupt sources.

Previously, the processing of the transmitted data checking was done by the microprocessor. The microprocessor relied on the traditional data checking service by waiting and comparing the transmitted data returned from a remote receiver with the transmitted data stored in the microprocessor memory. The processing of the traditional data checking took a great deal of the microprocessor time to perform bit-by-bit data checking and diminished the time available for the microprocessor for handling other important functions.

The real-time data error detection system with the enhancement of the bus cycle time helps free up the microprocessor and also reduces the software overhead when used in higher speed environment. The use of the real-time data error detection feature improves the overall system performance. The real-time data error detection feature is available in the SC28L201 Single (1-channel) UART and SC28L202 Dual (2-channel) UART, which are the Impact Line of Philips Semiconductors Industrial UARTs.

This application note describes the operation of the real-time data error detection feature and the process of the bit-by-bit real time error checking system. The enabling and programming of the feature and the mechanism of the real-time data error detection are discussed in Section 2 "Operation".

2. Operation

The real-time data error detection operation shown in Figure 1 and described below is mainly about the processing of the real-time error detection. The purpose of using the real-time data error detection feature is to give the user the flexibility and usability of performing bit-by-bit, real-time data transmission error checking for very high data integrity, especially in a long distance serial connection application.

As shown in Figure 1, the processor attached to the SC28L201/SC28L202 initiates the 8-bit parallel data transmission and the SC28L201/SC28L202 UART processes the parallel-to-serial data conversion. Then, the transmitter of SC28L201/SC28L202 UART stores and sends the serial data to the remote UART receiver. As soon as the data is received, the remote UART receiver will return it by sending it back to the SC28L201/SC28L202 UART via the remote UART transmitter. During its return, the data is received by the SC28L201/SC28L202 UART receiver and compared, about one bit-time later, with the stored data. The comparison is done on a byte boundary. Any errors identified by the real-time error detector during comparison immediately triggers the intelligent interrupt arbitration (I2A) system to generate an interrupt signal to the processor and the processor can retrieve the interrupt context provided by the interrupt arbitration

system to determine the errors. For more information about the I2A system, please visit this website http://www.standardics.philips.com/support/appnotes/datacom/ to retrieve the application note *AN10313, "Reduce CPU overhead with Intelligence Interrupt Arbitration (I2A) feature"*.

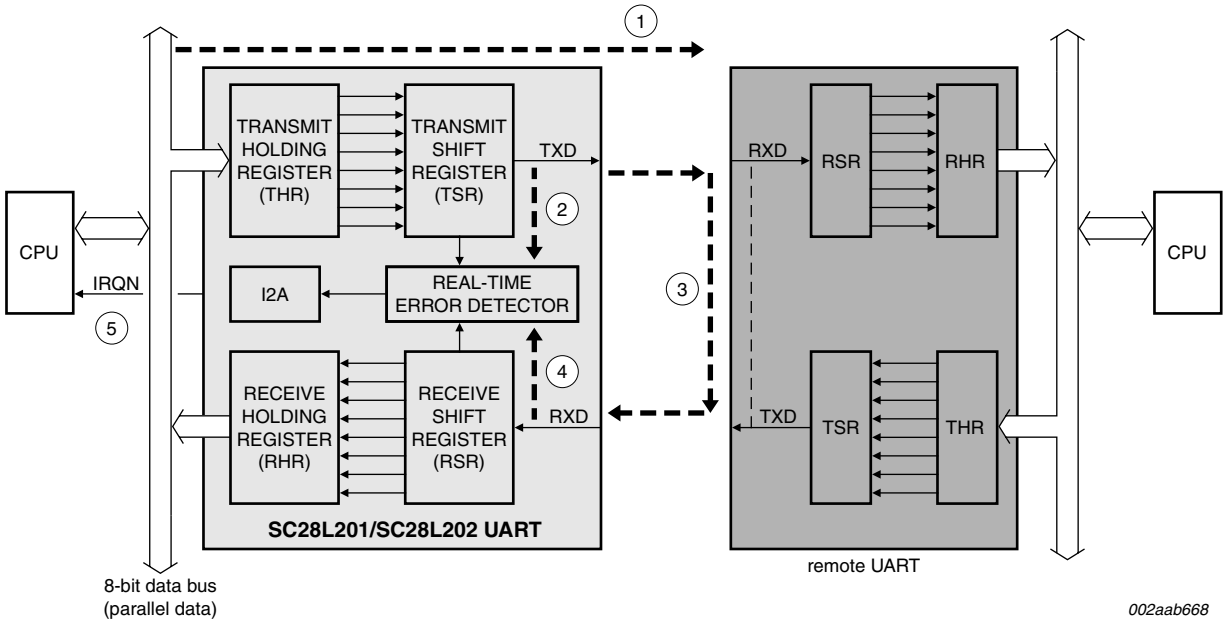

Fig 1. Real-time data error detection

The details of the data flow in the error checking processing is described as follows:

1. The CPU connected to the SC28L201/SC28L202 UART initiates the data flow.
2. After the parallel-to-serial conversion, the SC28L201/SC28L202 is storing the serial data while transmitting it.
3. As soon as the remote UART is receiving the data, the transmitter of the remote UART internally is triggered for sending it back to the SC28L201/SC28L202 UART.
4. While the SC28L201/SC28L202 UART is receiving the transmitted data, the real time data error detector is comparing it with the stored data.
5. If any mismatch data occurs, the interrupt arbitration (I2A) system will notify the CPU by generating the interrupt (IRQN) signal. Then, the CPU can retrieve the interrupt context in the Current Interrupt Register (CIR) provided by the I2A system.

The internal registers of SC28L201/SC28L202, which involves in the operation of the real-time data error detection, are SFSR (Special Feature and Status Register) or also called SFR (Special Function Register) and CIR (Current Interrupt Register). The detailed function of the internal registers in the error detection processing is described in Section 2.1 and Section 2.2.

2.1 SFSR: Special Feature and Status Register

The SFSR provides the status of loop back error check so the microprocessor can read the current status and find out if any errors occur during data comparison. Programming the SFSR bits (SFSR[2:1]) enables and disables the remote loop back error check function. If enabled, it sets an automatic error checking of the returned data. This mode stores the transmitted data, compares it to the data returned by the remote receiver, and generates an error status bit (SFSR[3]) which is read only for the processor to indicate the loop back error. The loop back error checking can be disabled by writing 00 to SFSR[2:1].

2.2 CIR: Current Interrupt Register

The CIR is provided to speed up the specification of the interrupting condition. It captures the value that is winning the interrupt arbitration and it is updated at the beginning of an interrupt acknowledge (IACKN) bus cycle or in response to an update CIR command. The contents remain in the CIR until another IACKN cycle or update CIR command occurs.

The CIR contains a complete description of the interrupting source, which contains the channel number, type of interrupt's source, and the fill level of FIFO. A single read operation to the CIR provides all the information needed to get the most common interrupt sources. For example, if the CIR[5:0] contains 001110, it indicates the receiver loop back error of channel A. Thus, the processor can read the contents of the CIR to determine the interrupt source. The value of the interrupting source in the CIR is used to drive the interrupt vector modification and the global interrupt registers, which are indirect address to the CIR.

3. Conclusion

The implementation of the real-time data error detection feature embedded in the Impact Line of Philips Semiconductors Industrial UARTs greatly reduces the microprocessor time required to service the UART data transmission error checking in real time. The error checking system allows the microprocessor to ensure very high data integrity and significantly reduce the microprocessor overhead of processing this task where certainty of transmission and reception is required.

4. Abbreviations

Table 1: Abbreviations

Acronym	Description
UART	Universal Asynchronous Receiver/Transmitter
I2A	Intelligent Interrupt Arbitration
CPU	Central Processing Unit
FIFO	First In, First Out

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7. Contents

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