

# APPLICATION NOTE

**ABSTRACT**

The objective of this application note is to show the specifics of Philips SC16C750 and the comparison to other industry standard 16C750. This application note is also applicable to Philips SC16C752.

## **AN10165** SC16C750 application note

Author: Dong Nguyen

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## SC16C750 application note

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The objective of this application note is to show the differences between Philips SC16C750 and other industry standard devices from TI. In most cases, the Philips SC16C750 is a direct drop-in replacement, but because software drivers vary from application to application, occasionally a minor software change may be required. This application note will point out areas to check if proper operation is not observed.

This application note is also applicable to Philips SC16C752.

### 1. READING THE ISR REGISTER

Whenever reading the ISR register, the LCR bit 7 must be set to 0.

### 2. HARDWARE FLOW CONTROL USING MCR BIT 5

Hardware flow control using MCR register bit 5 is not supported by Philips SC16C750. Hardware flow control is supported by another register called Enhanced Features Register (EFR) bit 7 and bit 6.

### 3. CLEARING OF TRANSMIT EMPTY INTERRUPT

If the transmit FIFO is empty and the interrupt on transmit FIFO empty is enabled (IER bit 1), the UART will generate a hardware interrupt. This hardware interrupt can be cleared by either reading the ISR register, or by writing a byte into the transmit FIFO. However, if the software does not write at least one byte into the transmit FIFO, then the transmit empty interrupt cannot be set again.

### 4. ADDITIONAL ENHANCED REGISTER

Our 16C750 device includes an enhanced register that is not available in the competitor devices. This extra register allows users to do auto hardware and software flow control (available on the TI16C752 only).

### 5. CLEARING RECEIVE INTERRUPT BY READING THE RECEIVE CHARACTER

If receive holding interrupt is enabled (IER register bit 0 = 1), upon receiving a character the UART will generate a receive interrupt. To clear this interrupt the software must read the ISR register and the received character.

### 6. DISABLE RECEIVE DATA TIMEOUT INTERRUPT

When the receive holding interrupt is enabled (IER bit 0 = 1), and the receiver receives a number of characters, the software must read the receive FIFO before the receive timeout interrupt is generated (refer to the data sheet to calculate the timeout). If the receive timeout interrupt is generated, the software must read all the data in the receive FIFO before disabling the receive ready interrupt.

### 7. SETTING TCR REGISTER (SC16C752 ONLY)

If the TCR register is used to set-up the trigger levels for hardware or software flow control, FCR register bit [7:6] must be set to a value other than 11b. Otherwise the receiver will continuously send out garbage data once the  $\overline{\text{RTS}}$  signal is negated or XOFF control character has been sent.

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## Digital DataComm

Web address: [www.philipslogic.com](http://www.philipslogic.com)Email address: [DataCom.tech-support@philips.com](mailto:DataCom.tech-support@philips.com)

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### Contact information

For additional information please visit  
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

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