

# Bus Repeaters Expand Use Of Popular Inter-IC Bus

Rather than accept that it has reached the end of its life, the venerable I<sup>2</sup>C bus has regained momentum as bus repeaters extend its capabilities.



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Continued interest in the decades-old serial inter-IC bus (I<sup>2</sup>C) prompted its creator, Royal Philips Electronics, to develop a family of bus repeaters that can double the number of devices able to reside on the same bus system (from 20 to 30 devices up to 40 to 60 devices). With the expanded use of the I<sup>2</sup>C as a maintenance and control bus, such as the



SMBus in computing, telecommunications, and networking systems, these repeater chips will let designers build larger I<sup>2</sup>C systems than currently possible. The chips will also permit the hot-swapping of I<sup>2</sup>C cards into an active system.

Three repeater chips will initially be offered: the PCA9515, 9516, and 9518. The

PCA9515 is a single repeater in an eight-lead package. It will support up to 800 pF of capacitive loading by splitting the bus into two segments. Both the 9516 and 9518 contain four repeaters, each with individual enable pins. These chips can be used like a hub, enabling the main I<sup>2</sup>C bus to send signals to four downstream I<sup>2</sup>C buses.

Available in a 16-lead package, the 9516 is limited to the four downstream ports. The 9518 comes in a larger 20-lead package. Its expansion interface allows multiple repeaters to be concatenated, so an almost unlimited number of bus segments can be added. The hub device includes bidirectional I<sup>2</sup>C drivers that isolate the bus capacitance on each segment. The hubs are multi-master-capable, which means that the repeater is transparent to bus arbitration and contention protocols. They have only one repeater delay between segments.

All three devices allow voltage translation, with either 3.3 or 5 V on any of the I<sup>2</sup>C sub-branches. The repeaters are available in both SO and space-saving TSSOP packages. The PCA9515, 9516, and 9518 cost \$0.78, \$1.08, and \$1.20, respectively, in 10,000-unit lots. An evaluation board connects to a PC's parallel port and includes a simple to use graphical user interface. Samples and production quantities are immediately available.

#### Philips Semiconductors

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## HOT PRODUCT

### Low-Cost ARM-Based Microcontrollers Maintain Powerful Edge

The small-sized 32-bit ARM CPU core, coupled with a suite of on-chip peripherals and flash memory, has let OKI craft a new family of low-cost, general-purpose microcontrollers. Priced competitively with some high-end 8- and 16-bit MCUs, the ARM-based chips establish a new price/performance point for 32-bit embedded processors. The ML674001, MLQ674002, and MLQ674003 combine the ARM7TDMI core along with a broad array of peripheral functions.



Although the ML674001 contains no flash memory, like the other family members, it includes 32 kbytes of SRAM, a boot ROM, a four-channel 10-bit ADC, seven 16-bit timers, a dual-stage 16-bit watchdog timer, two DMA channels, and two 16-bit pulse-width modulated channels. It also incorporates up to 43 pins of general-purpose I/O, multiple serial interfaces (SIO, UART, USART, and I<sup>2</sup>C), 28 interrupt sources, and a memory controller to support external SDRAM and other memory types.

The controllers can operate at 33 MHz from -40°C to 85°C. Because the core is a member of the ARM family, all software-development tools for the ARM can be used to develop application software for this family of MCUs.

In 10,000-unit lots, the flashless ML674001 costs less than \$5, the 256-kbyte MLQ674002, costs from \$6 to \$7, and the 512-kbyte MLQ674003 costs under \$8. Samples are available from stock.

#### OKI Semiconductor

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## BREAKING NEWS

**>NEXT-GENERATION ITANIUM CPU DELIVERS 30% TO 50% HIGHER THROUGHPUT THAN ITS PREDECESSOR With 6 Mbytes of cache and a clock speed jump of 50% to 1.5 GHz, Intel's latest Itanium2 processor (Madison) delivers 30% to 50% more throughput than the current version (McKinley). Described at last month's International Solid State Circuits Conference, the CPU was fabricated using 130-nm design rules and uses a 1.3-V supply so it can stay within the 130-W power envelope established for the Itanium CPUs. Because it will have the same pinout and 400-MHz front-side bus as the previous CPU, designers can quickly upgrade CPU boards to use the latest processors. Intel plans to offer several versions of the Itanium2 CPU. Versions will differ in the amount of on-chip cache and clock speed. Cache options will include 3, 4, or 6 Mbytes. Future plans call for a larger cache—9 Mbytes—in 2004 (Deerfield CPU), which will raise the transistor count on the CPU to over 500 million devices. Planned for release in 2005, the Montecito processor will contain two full CPUs, each with its own level 3 cache, and a bus arbiter. For more, go to [www.intel.com](http://www.intel.com).**