

# 74LV74

Dual D-type flip-flop with set and reset; positive edge-trigger

Rev. 03 — 28 September 2007

Product data sheet

## 1. General description

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The 74LV74 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC74 and 74HCT74.

The device is a dual positive edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ( $\overline{SD}$ ) and ( $\overline{RD}$ ) inputs, and complementary Q and  $\overline{Q}$  outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt trigger action in the clock input makes the circuit highly tolerant of slower clock rise and fall times.

## 2. Features

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- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical output ground bounce < 0.8 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical output  $V_{OH}$  undershoot > 2 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and from  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LV74N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV74D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV74DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV74PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV74PW	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram

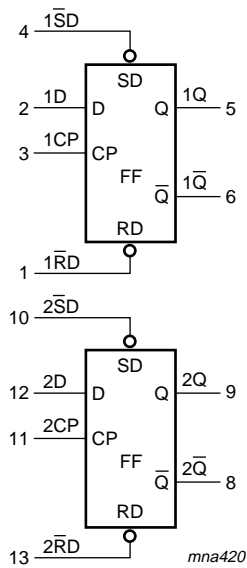


Fig 1. Logic symbol

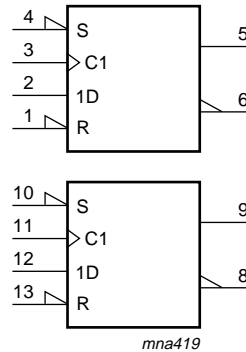
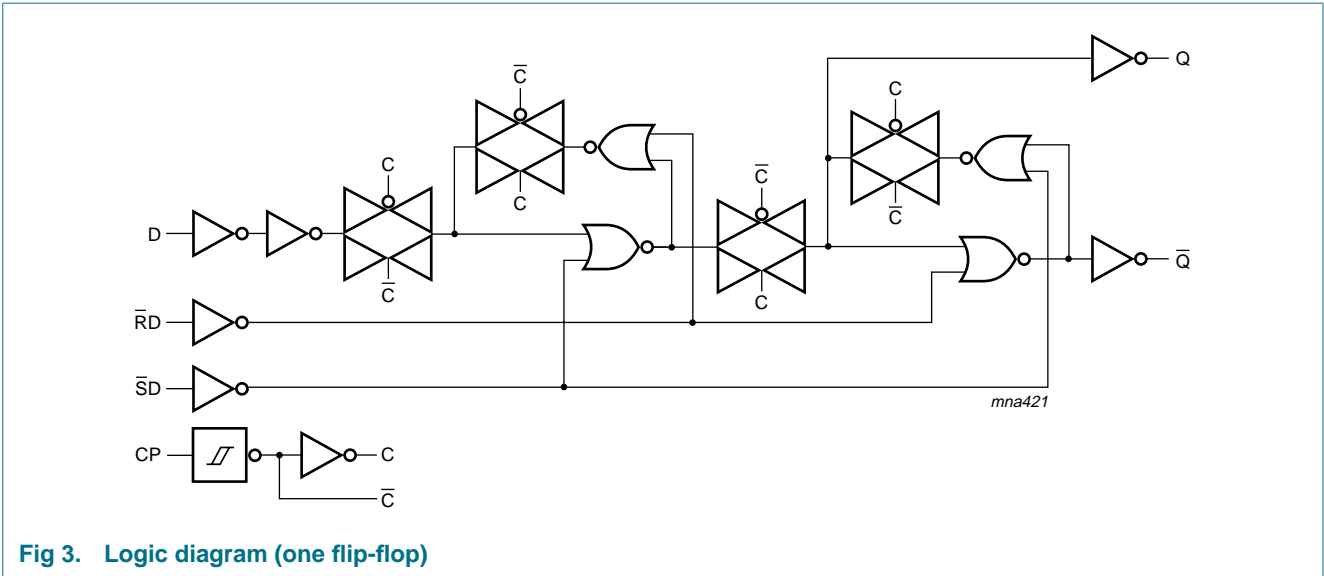
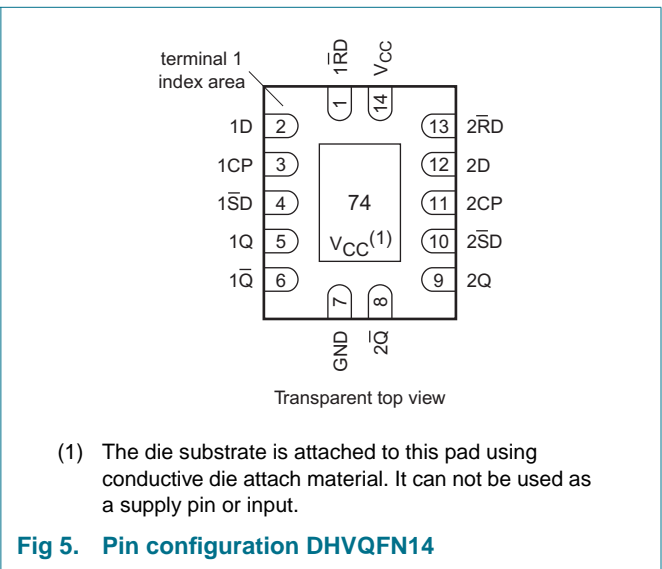
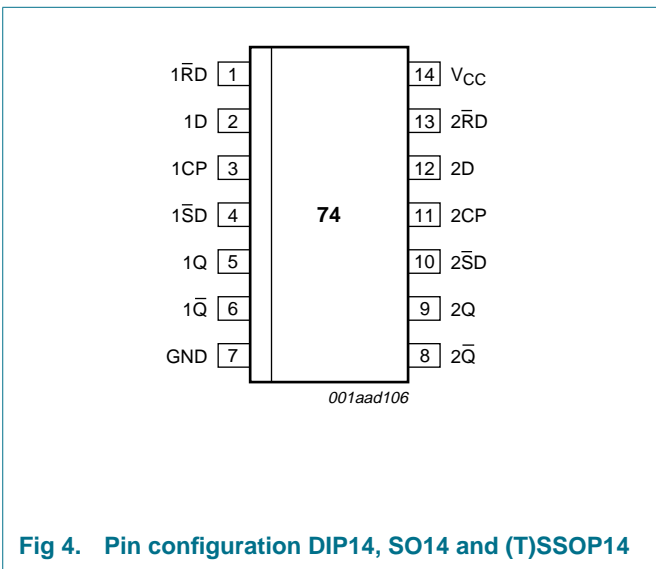


Fig 2. IEC logic symbol



## 5. Pinning information

### 5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol (n = 1, 2)	Pin	Description
$\overline{nRD}$	1, 13	asynchronous reset-direct input (active LOW)
nD	2, 12	data input
nCP	3, 11	clock input (LOW-to-HIGH, edge-triggered)
$\overline{nSD}$	4, 10	asynchronous set-direct input (active LOW)
nQ	5, 9	true flip-flop output
$\overline{nQ}$	6, 8	complement flip-flop output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs				Outputs	
$\overline{nSD}$	$\overline{nRD}$	nCP	nD	nQ	$\overline{nQ}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

Table 4. Function table<sup>[1]</sup>

Inputs				Outputs	
$\overline{nSD}$	$\overline{nRD}$	nCP	nD	nQ <sub>n+1</sub>	$\overline{nQ}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level  
 ↑ = LOW-to-HIGH transition  
 Q<sub>n+1</sub> = state after the next LOW-to-HIGH CP transition

## 7. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	±50	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	±25	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		DIP14 package	[2] -	750	mW
		SO14 package	[3] -	500	mW
		(T)SSOP14 package	[4] -	500	mW
		DHVQFN14 package	[5] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[3]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

[4]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

[5]  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage[1]		1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate[2]	$V_{CC} = 1.0\text{ V}$ to $2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to $2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V}$ to $5.5\text{ V}$	-	-	50	ns/V

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 5.5\text{ V}$ , but LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

[2] Except for clock inputs, which have Schmitt trigger action..

## 9. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.2 V	-	1.2	-	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V	2.5	2.7	-	2.5	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 3.0 V	2.8	3.0	-	2.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 4.5 V	4.3	4.5	-	4.3	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 3.0 V	2.4	2.82	-	2.2	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 4.5 V	3.6	4.2	-	3.5	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 3.0 V	-	0.25	0.40	-	0.50	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**  
*GND = 0 V; For test circuit see [Figure 8](#).*

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$t_{pd}$	propagation delay	nCP to nQ, n $\bar{Q}$ ; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		$V_{CC} = 1.2\text{ V}$	-	70	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	24	44	-	56	ns
		$V_{CC} = 2.7\text{ V}$	-	18	28	-	41	ns
		$V_{CC} = 3.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	11	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ <sup>[3]</sup>	-	13	26	-	33	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ <sup>[3]</sup>	-	9.5	17	-	23	ns
		n $\bar{S}D$ to nQ, n $\bar{Q}$ ; n $\bar{R}D$ to nQ, n $\bar{Q}$ ; see <a href="#">Figure 7</a>						
		$V_{CC} = 1.2\text{ V}$	-	90	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	31	46	-	58	ns
		$V_{CC} = 2.7\text{ V}$	-	23	34	-	43	ns
		$V_{CC} = 3.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	14	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ <sup>[3]</sup>	-	17	27	-	34	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ <sup>[3]</sup>	-	12	19	-	24	ns
$t_W$	pulse width	clock HIGH or LOW; see <a href="#">Figure 6</a> ; set or reset LOW; see <a href="#">Figure 7</a>						
		$V_{CC} = 2.0\text{ V}$	34	10	-	41	-	ns
		$V_{CC} = 2.7\text{ V}$	25	8	-	30	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ <sup>[3]</sup>	20	7	-	24	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ <sup>[3]</sup>	15	6	-	18	-	ns
$t_{rec}$	recovery time	set or reset; see <a href="#">Figure 7</a>						
		$V_{CC} = 1.2\text{ V}$	-	5	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	14	2	-	15	-	ns
		$V_{CC} = 2.7\text{ V}$	10	1	-	11	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ <sup>[3]</sup>	8	1	-	9	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ <sup>[3]</sup>	6	1	-	7	-	ns
$t_{su}$	set-up time	nD to nCP; see <a href="#">Figure 6</a>						
		$V_{CC} = 1.2\text{ V}$	-	10	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	22	4	-	26	-	ns
		$V_{CC} = 2.7\text{ V}$	12	3	-	15	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ <sup>[3]</sup>	8	2	-	10	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ <sup>[3]</sup>	6	1	-	8	-	ns

**Table 8. Dynamic characteristics ...continued**

$GND = 0\text{ V}$ ; For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max		
$t_h$	hold time	nD to nCP; see <a href="#">Figure 6</a>							
		$V_{CC} = 1.2\text{ V}$	-	-10	-	-	-	ns	
		$V_{CC} = 2.0\text{ V}$	3	-2	-	3	-	ns	
		$V_{CC} = 2.7\text{ V}$	3	-2	-	3	-	ns	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	<a href="#">[3]</a>	3	-2	-	3	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	<a href="#">[3]</a>	3	-2	-	3	-	ns
$f_{max}$	maximum frequency	see <a href="#">Figure 6</a>							
		$V_{CC} = 2.0\text{ V}$	14	40	-	12	-	MHz	
		$V_{CC} = 2.7\text{ V}$	50	90	-	40	-	MHz	
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	76	-	-	-	MHz	
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	<a href="#">[3]</a>	60	100	-	48	-	MHz
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	<a href="#">[3]</a>	70	110	-	56	-	MHz
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_I = GND\text{ to }V_{CC}$	<a href="#">[4]</a>	-	24	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 5.0\text{ V}$ ).

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

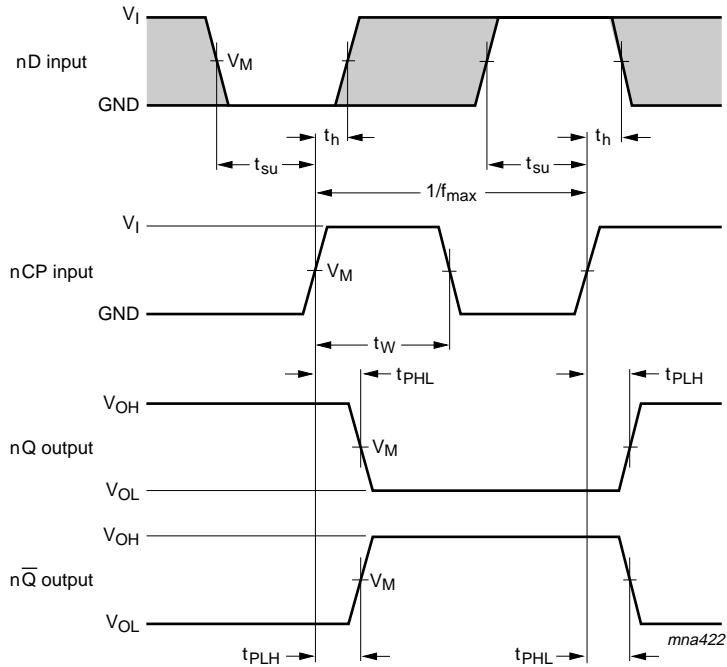
$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in Volts

$N$  = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

11. Waveforms

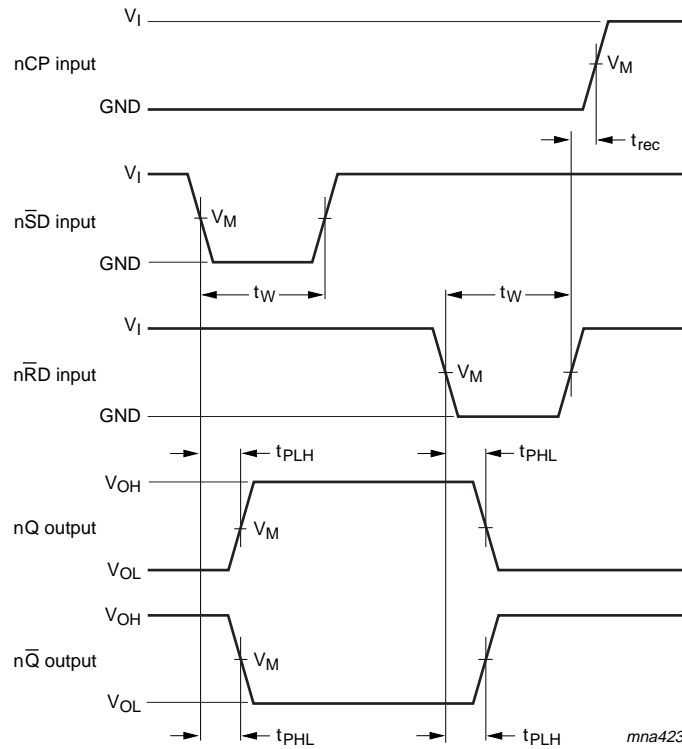


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in [Table 9](#).

VOH and VOL are typical output voltage drops that occur with the output load.

**Fig 6.** The clock input (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, and the maximum frequency



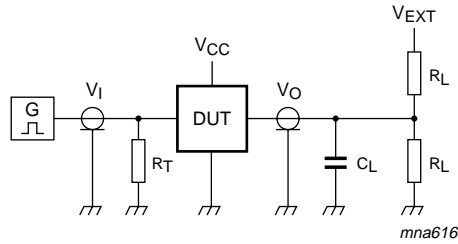
Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage drops that occur with the output load.

**Fig 7. The set ( $n\overline{SD}$ ) and reset ( $n\overline{RD}$ ) input to output ( $nQ$ ,  $n\overline{Q}$ ) propagation delays, the set and reset pulse widths, and the  $n\overline{RD}$  to  $n\overline{CP}$  recovery time**

**Table 9. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
$\geq 4.5$ V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 10](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 8. Load circuit for switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$
$\geq 4.5$ V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

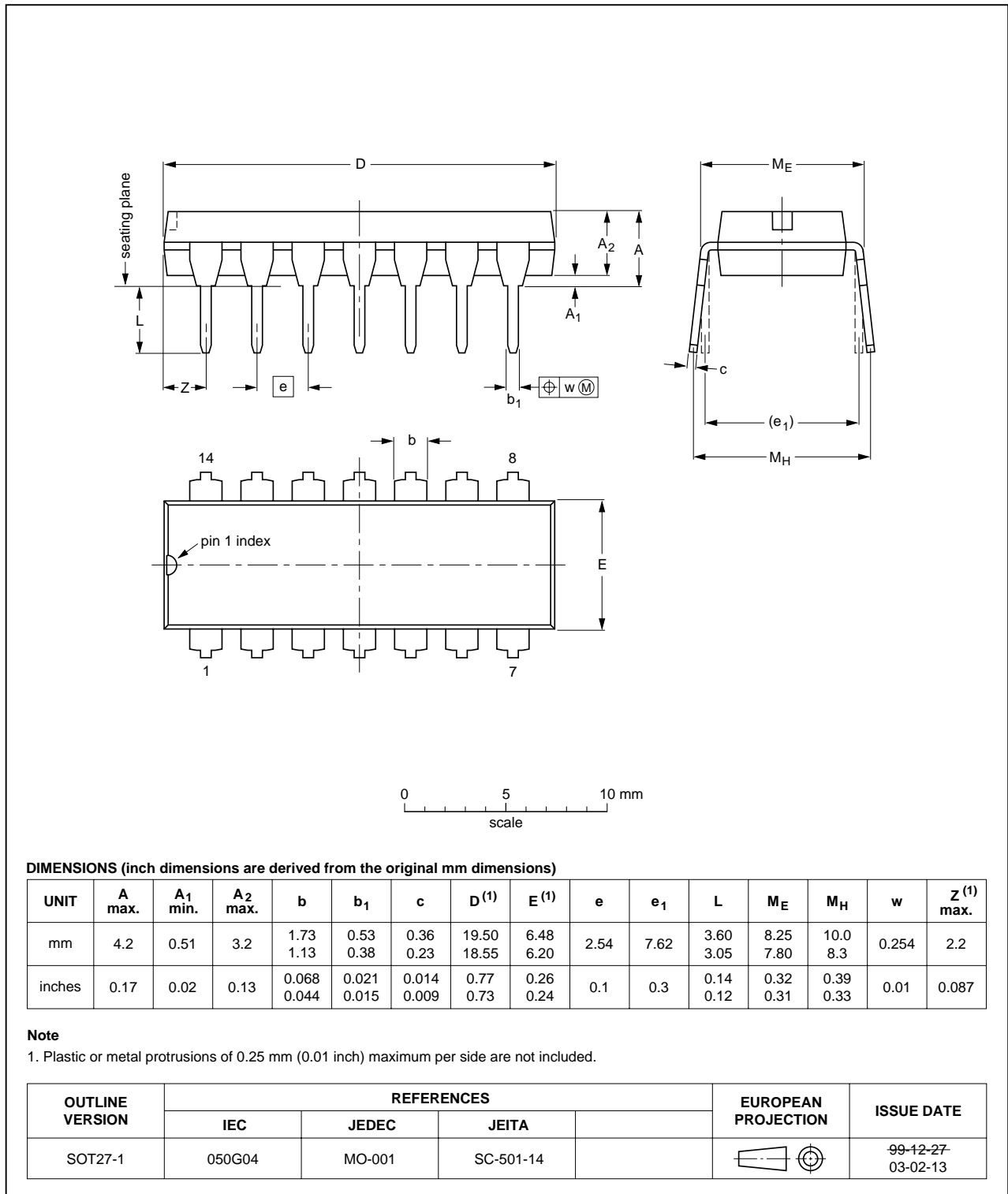


Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

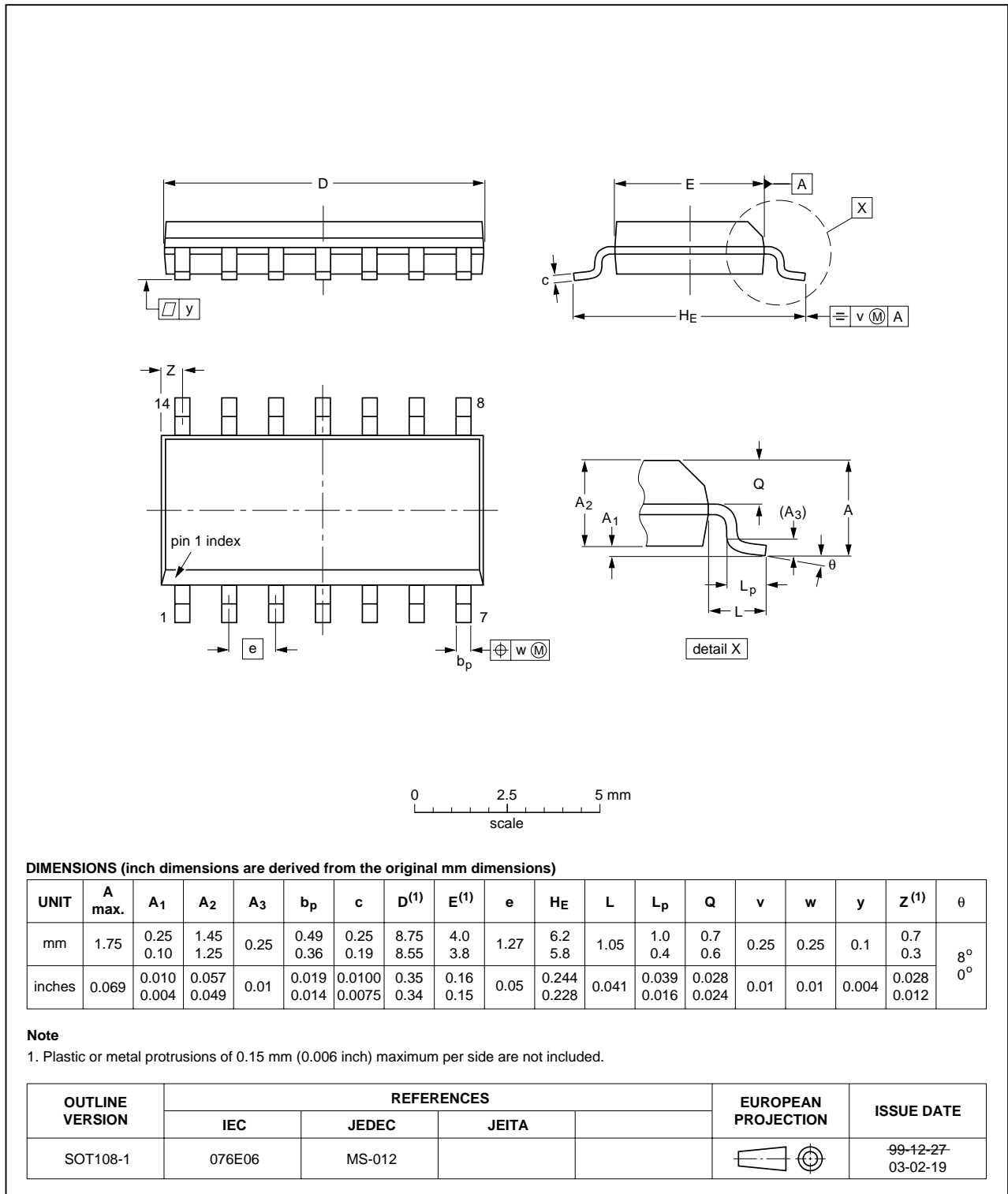


Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

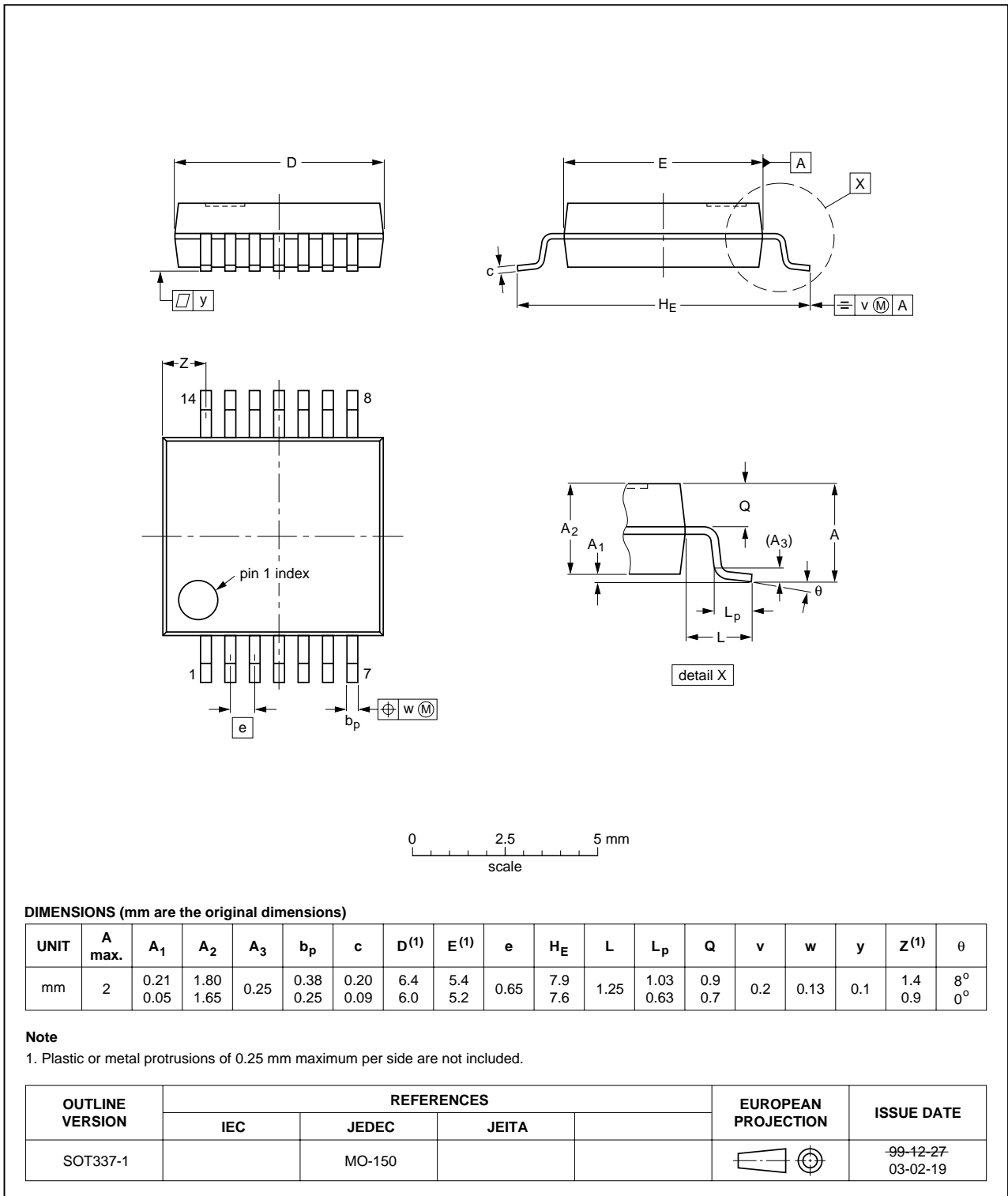


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

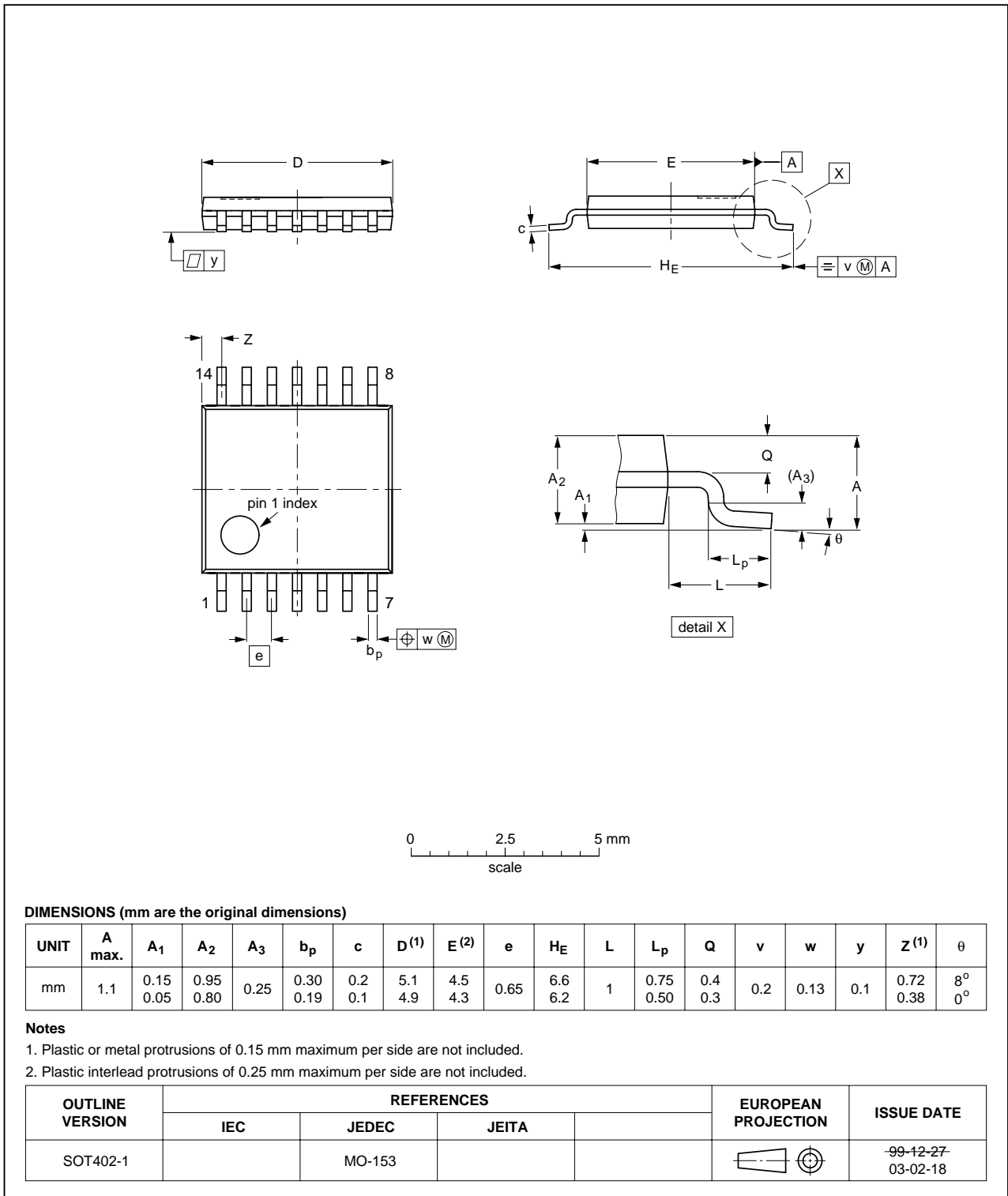


Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

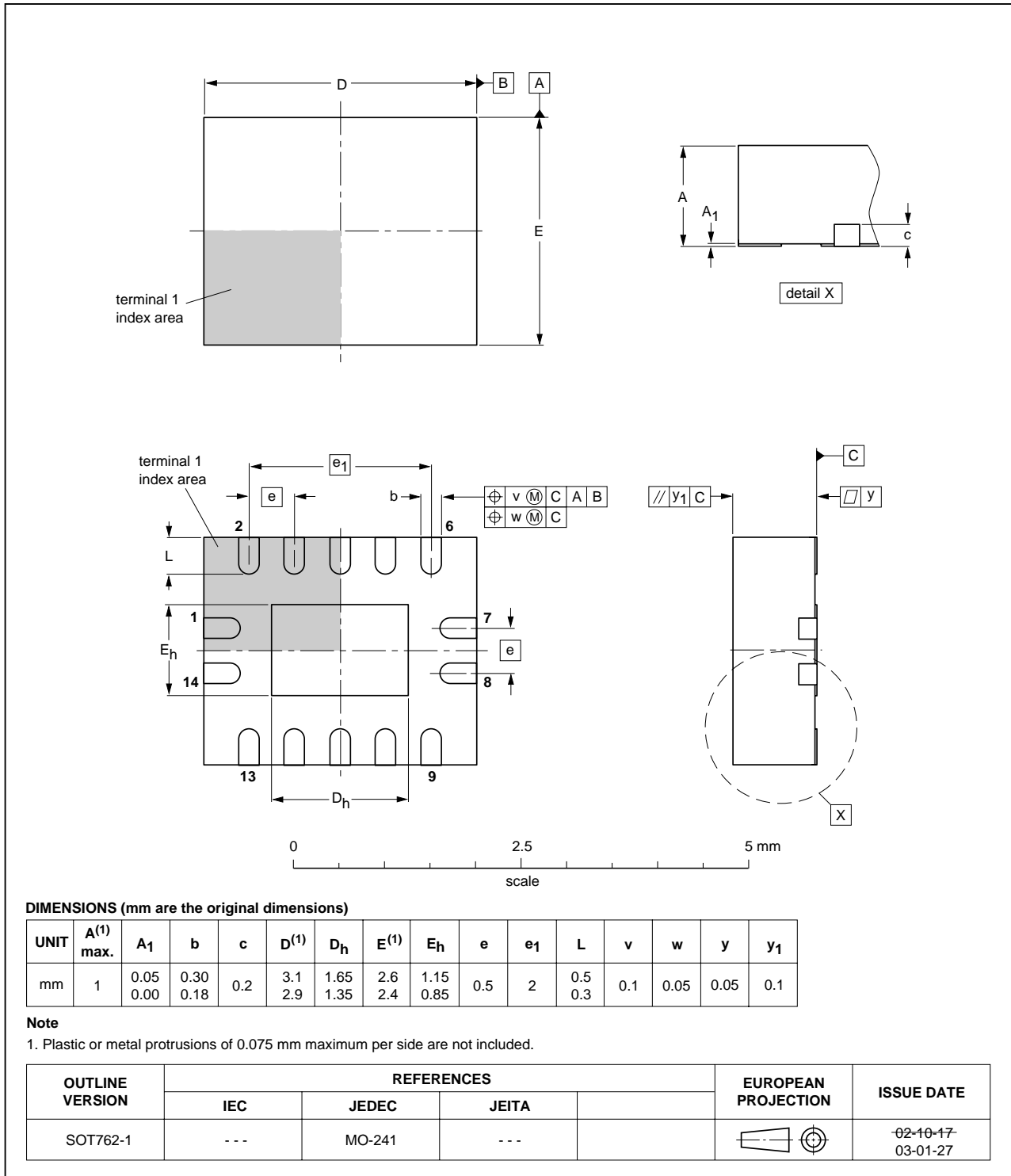


Fig 13. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV74_3	20070928	Product data sheet	-	74LV74_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name when appropriate.</li> <li><a href="#">Section 3</a>: DHVQFN14package added.</li> <li><a href="#">Section 7</a>: derating values added for DHVQFN14 package.</li> <li><a href="#">Section 12</a>: outline drawing added for DHVQFN14 package.</li> </ul>			
74LV74_2	19980420	Product specification	-	74LV74_1
74LV74_1	19961107	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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