

74HC2G126; 74HCT2G126

Dual buffer/line driver; 3-state

Rev. 03 — 7 May 2009

Product data sheet

1. General description

The 74HC2G126; 74HCT2G126 is a high-speed Si-gate CMOS device.

The 74HC2G126; 74HCT2G126 provides two non-inverting buffer/line drivers with 3-state output. The 3-state output is controlled by the output enable input pin (OE). A LOW at pin OE causes the output to assume a high-impedance OFF-state.

The bus driver output currents are equal compared to the 74HC126 and 74HCT126.

2. Features

- Wide operating voltage from 2.0 V to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC2G126DP 74HCT2G126DP	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HC2G126DC 74HCT2G126DC	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HC2G126GD 74HCT2G126GD	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body $3 \times 2 \times 0.5\text{ mm}$	SOT996-2

4. Functional diagram

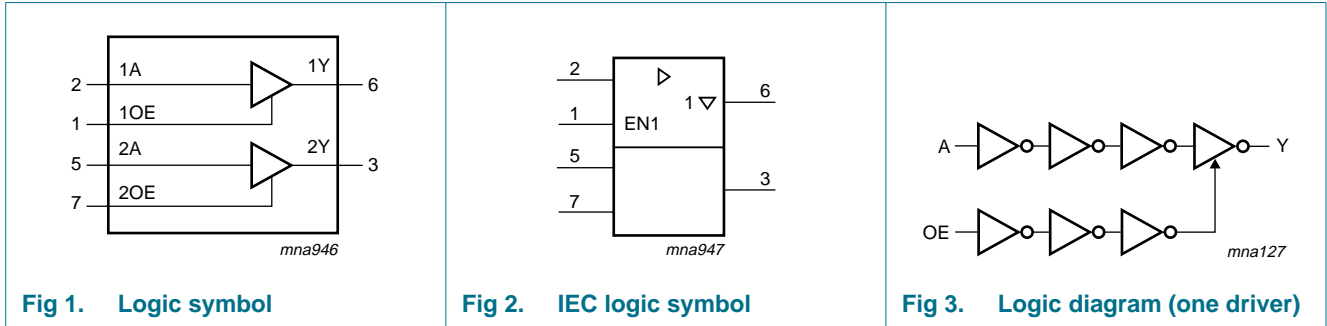


Fig 1. Logic symbol

Fig 2. IEC logic symbol

Fig 3. Logic diagram (one driver)

5. Pinning information

5.1 Pinning

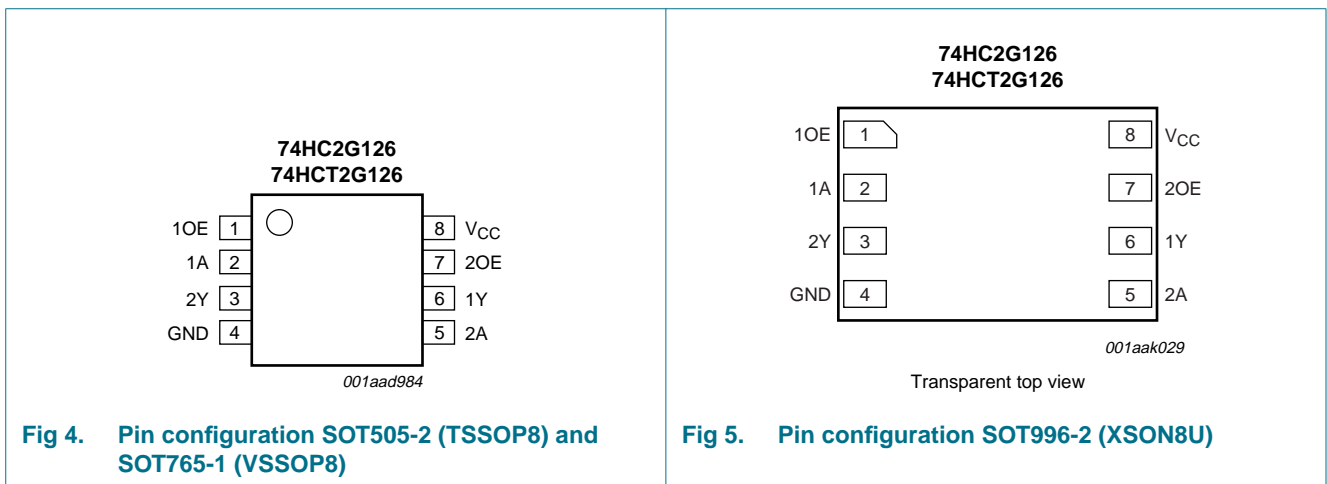


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

Fig 5. Pin configuration SOT996-2 (XSON8U)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 7	output enable input
1A, 2A	2, 5	data input
1Y, 2Y	6, 3	data output
GND	4	ground (0 V)
V _{CC}	8	supply voltage

6. Functional description

Table 3. Function table^[1]

Input		Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1] -	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1] -	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	[1] -	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		[2] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

For XSON8U package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G126			74HCT2G126			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ	Max	Min	Max	
74HC2G126								
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or } V_{IL}$						
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	V
		$I_O = -6.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.84	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or } V_{IL}$						
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	V
		$I_O = 6.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 6.0\text{ V}$	-	-	± 1.0	-	± 1.0	μA
		$V_I = V_{IH}\text{ or } V_{IL}; V_O = V_{CC}\text{ or GND}; V_{CC} = 6.0\text{ V}$	-	-	± 5.0	-	± 10	μA
I_{CC}	supply current	$V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}; V_{CC} = 6.0\text{ V}$	-	-	10	-	20	μA
C_I	input capacitance		-	1.0	-	-	-	pF
C_O	output capacitance		-	1.5	-	-	-	pF
74HCT2G126								
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	-	1.2	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or } V_{IL}; V_{CC} = 4.5\text{ V}$						
		$I_O = -20\text{ }\mu\text{A}$	4.4	4.5	-	4.4	-	V
		$I_O = -6.0\text{ mA}$	3.84	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or } V_{IL}; V_{CC} = 4.5\text{ V}$						
		$I_O = 20\text{ }\mu\text{A}$	-	0	0.1	-	0.1	V
		$I_O = 6.0\text{ mA}$	-	0.16	0.33	-	0.4	V

Table 6. Static characteristics ...continued

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	± 1.0	-	± 1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	± 5.0	-	± 10	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 5.5\text{ V}$	-	-	10	-	20	μA
ΔI_{CC}	additional supply current	per input; $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$; $V_I = V_{CC} - 2.1\text{ V}$; $I_O = 0\text{ A}$	-	-	375	-	410	μA
C_I	input capacitance		-	1.0	-	-	-	pF
C_O	output capacitance		-	1.5	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50\text{ pF}$ unless otherwise specified; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HC2G126								
t_{pd}	propagation delay	nA to nY; see Figure 6 ^[2]						
		$V_{CC} = 2.0\text{ V}$	-	35	115	-	135	ns
		$V_{CC} = 4.5\text{ V}$	-	11	23	-	27	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	10	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	8	20	-	23	ns
t_{en}	enable time	nOE to nY; see Figure 7 ^[2]						
		$V_{CC} = 2.0\text{ V}$	-	40	115	-	135	ns
		$V_{CC} = 4.5\text{ V}$	-	11	23	-	27	ns
		$V_{CC} = 6.0\text{ V}$	-	8	20	-	23	ns
t_{dis}	disable time	nOE to nY; see Figure 7 ^[2]						
		$V_{CC} = 2.0\text{ V}$	-	25	125	-	150	ns
		$V_{CC} = 4.5\text{ V}$	-	12	25	-	30	ns
		$V_{CC} = 6.0\text{ V}$	-	10	21	-	26	ns
t_t	transition time	nY; see Figure 6 ^[2]						
		$V_{CC} = 2.0\text{ V}$	-	18	75	-	90	ns
		$V_{CC} = 4.5\text{ V}$	-	6	15	-	18	ns
		$V_{CC} = 6.0\text{ V}$	-	5	13	-	15	ns
C_{PD}	power dissipation capacitance	per buffer; $V_I = \text{GND to } V_{CC}$ ^[3]						
		output enabled	-	11	-	-	-	pF
		output disabled	-	1	-	-	-	pF

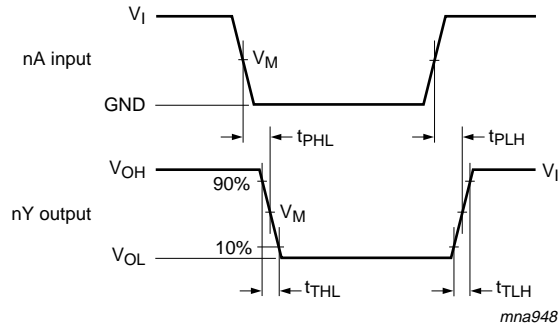
Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit		
			Min	Typ ^[1]	Max	Min	Max			
74HCT2G126										
t _{pd}	propagation delay	nA to nY; see Figure 6		[2]						
		V _{CC} = 4.5 V	-	15	30	-	36	ns		
		V _{CC} = 5.0 V; C _L = 15 pF	-	12	-	-	-	ns		
t _{en}	enable time	nOE to nY; see Figure 7 ; V _{CC} = 4.5 V		[2]	-	11	31	-	38	ns
t _{dis}	disable time	nOE to nY; see Figure 7 ; V _{CC} = 4.5 V		[2]	-	11	35	-	42	ns
t _t	transition time	nY; see Figure 6 ; V _{CC} = 4.5 V		[2]	-	6	15	-	18	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} - 1.5 V		[3]						
		output enabled	-	11	-	-	-	-	pF	
		output disabled	-	1	-	-	-	-	pF	

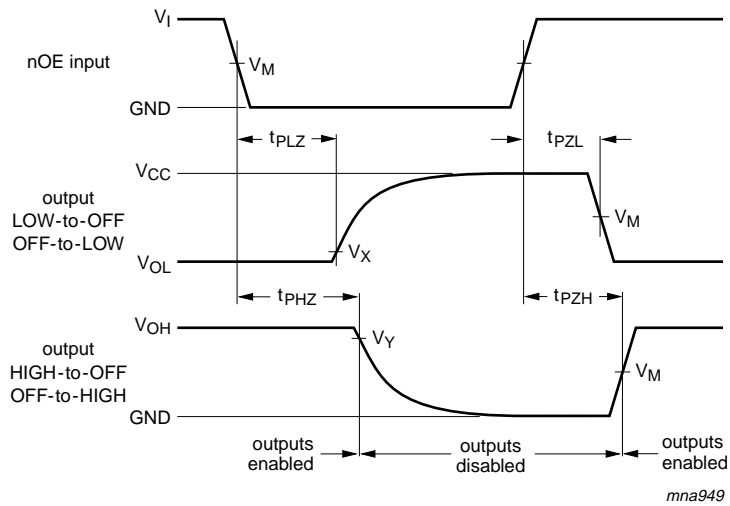
- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of outputs.

11. Waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (nA) to output (nY) and transition time output (nY)



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC2G126	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
74HCT2G126	1.3 V	1.3 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

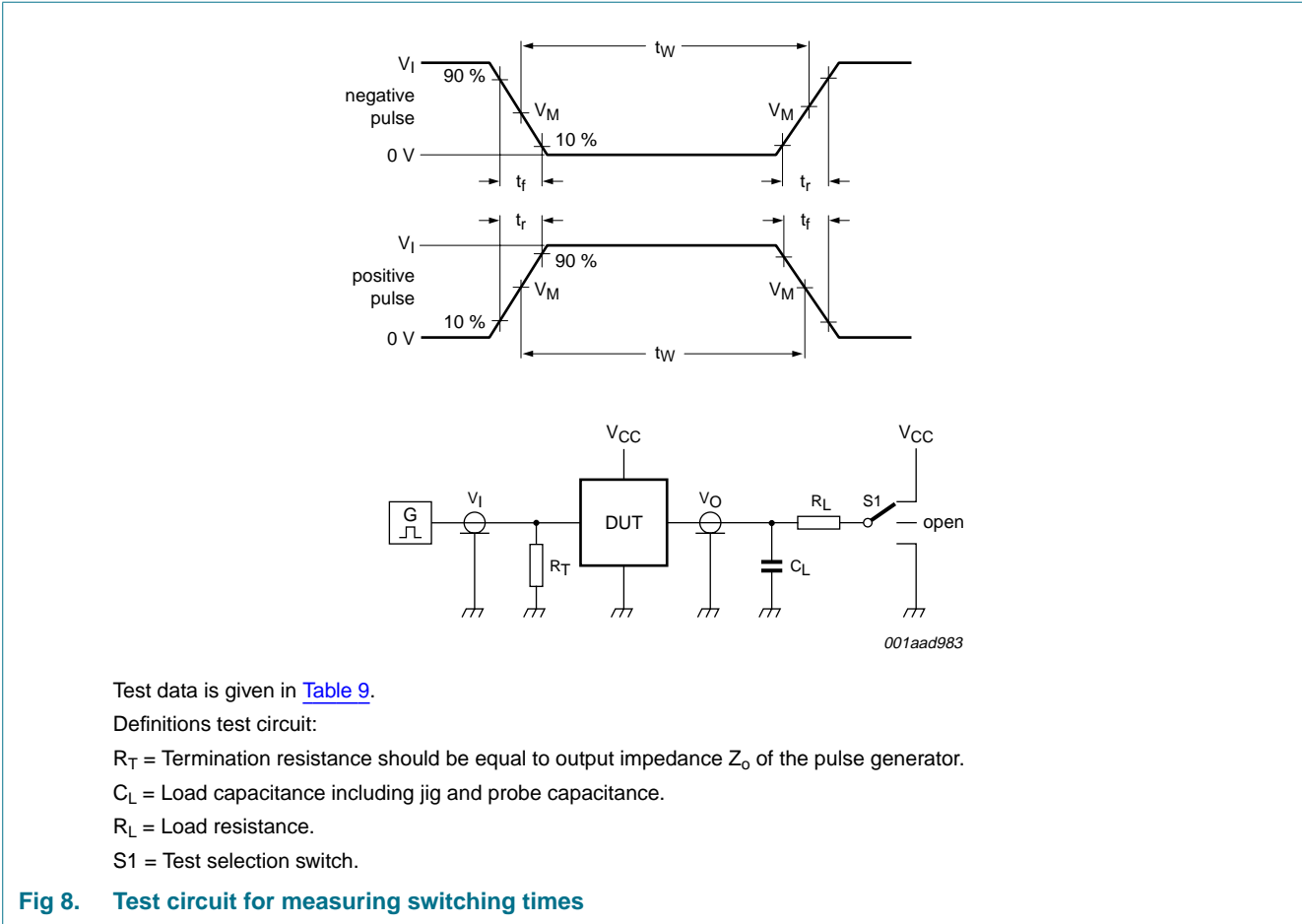


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC2G126	GND to V_{CC}	≤ 6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT2G126	GND to 3 V	≤ 6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

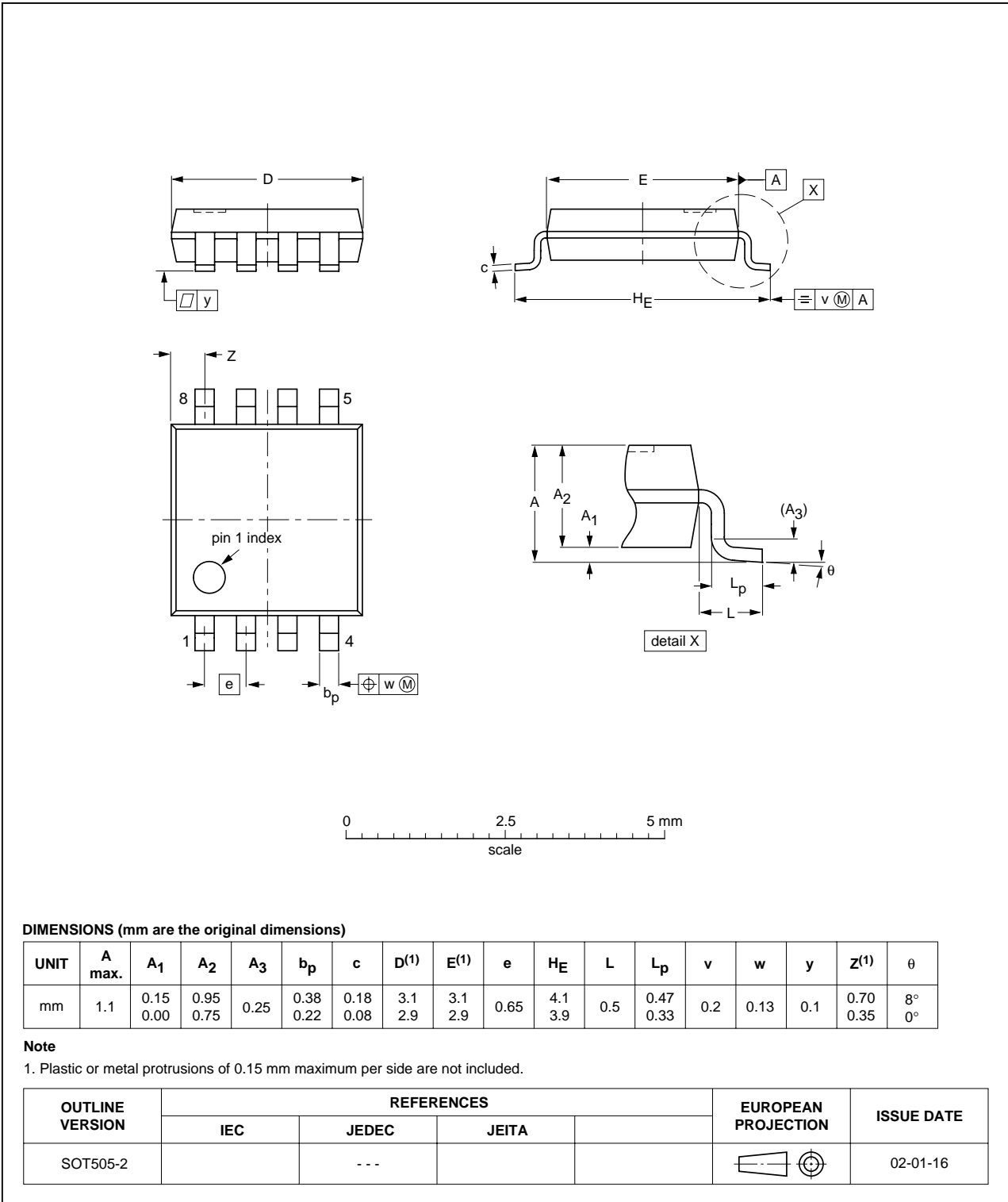


Fig 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

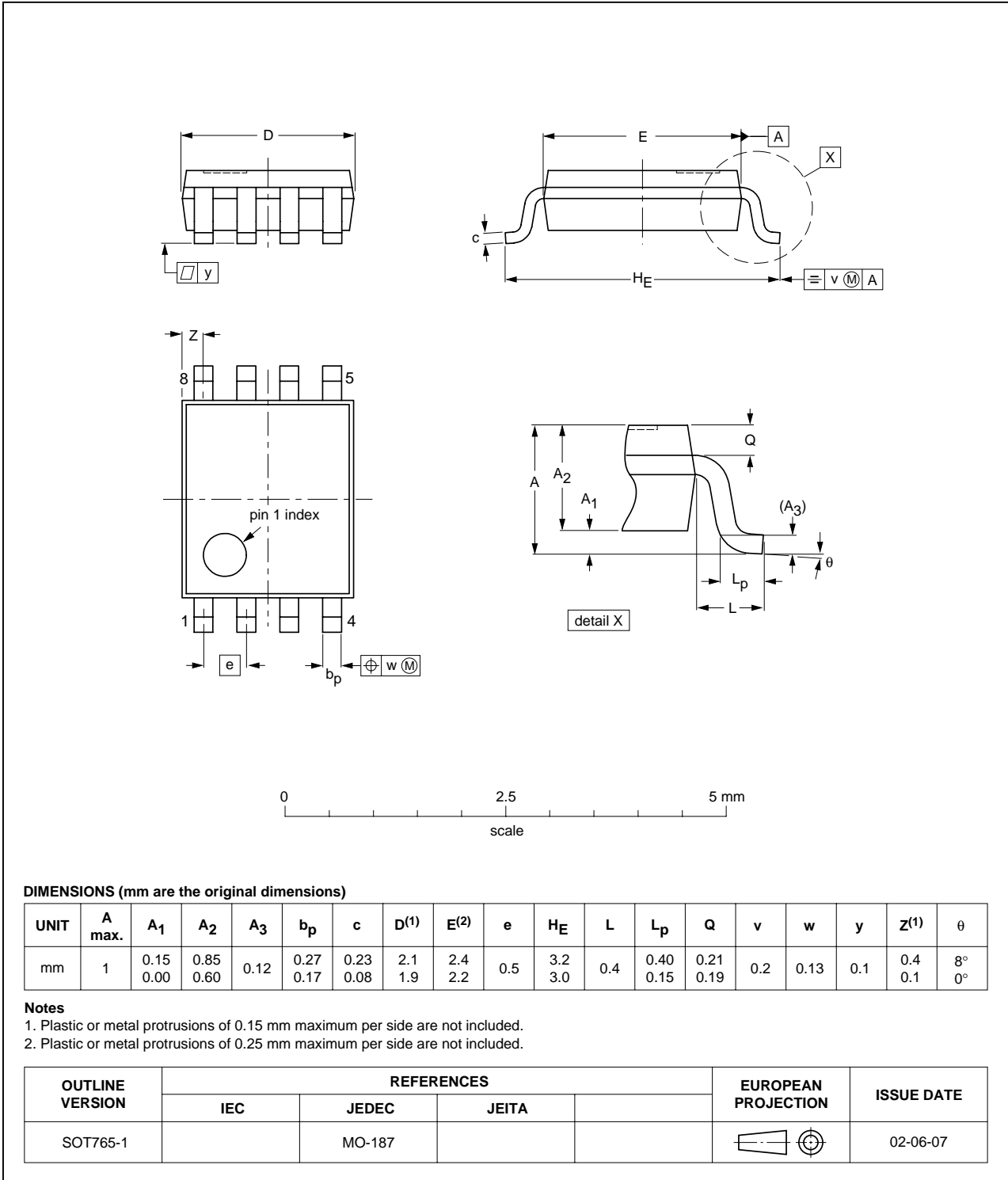


Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8U: plastic extremely thin small outline package; no leads;
8 terminals; UTLP based; body 3 x 2 x 0.5 mm

SOT996-2

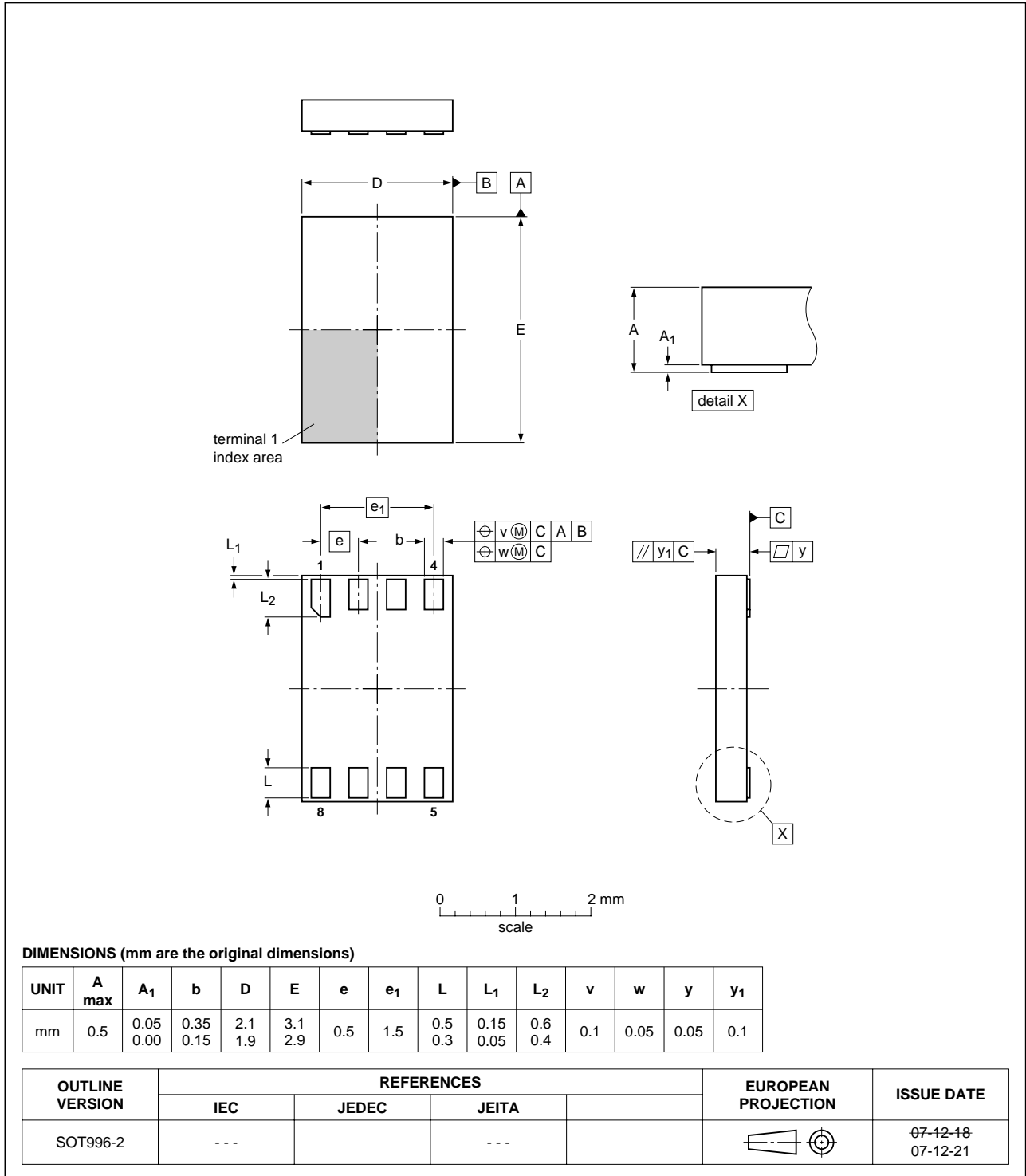


Fig 11. Package outline SOT996-2 (XSON8U)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G126_3	20090507	Product data sheet	-	74HC_HCT2G126_2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Quick reference data removed Added type numbers 74HC2G126GD and 74HCT2G126GD (XSON8U package) Section 7: derating factor for TSSOP8, VSSOP8 and XSON8U package added 			
74HC_HCT2G126_2	20051215	Product data sheet	-	74HC_HCT2G126_1
74HC_HCT2G126_1	20030303	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	2
5.1	Pinning	2
5.2	Pin description	2
6	Functional description	3
7	Limiting values	3
8	Recommended operating conditions	3
9	Static characteristics	4
10	Dynamic characteristics	5
11	Waveforms	7
12	Package outline	9
13	Abbreviations	12
14	Revision history	12
15	Legal information	13
15.1	Data sheet status	13
15.2	Definitions	13
15.3	Disclaimers	13
15.4	Trademarks	13
16	Contact information	13
17	Contents	14

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 7 May 2009

Document identifier: 74HC_HCT2G126_3