

DATA SHEET

74ABT16821A

74ABTH16821A

20-bit bus-interface D-type flip-flop;
positive-edge trigger (3-State)

Product data
Supersedes data of 1998 Feb 27

2002 Dec 13

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

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FEATURES

- 20-bit positive-edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- 74ABTH16821A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64 mA / -32 mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16821A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16821A has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (nOE) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active-LOW Output Enable (nOE) controls all ten 3-State buffers independent of the register operation. When nOE is LOW, the data in the register appears at the outputs. When nOE is HIGH, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

Two options are available, 74ABT16821A which does not have the bus-hold feature and 74ABTH16821A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}; \text{GND} = 0\text{ V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	$C_L = 50\text{ pF}; V_{CC} = 5\text{ V}$	2.4 2.0	ns
C_{IN}	Input capacitance	$V_I = 0\text{ V or } V_{CC}$	3	pF
C_{OUT}	Output capacitance	$V_O = 0\text{ V or } V_{CC}; \text{3-State}$	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	500	μA
I_{CCL}		Outputs LOW; $V_{CC} = 5.5\text{ V}$	10	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
56-Pin Plastic SSOP Type III	-40 °C to +85 °C	74ABT16821ADL	SOT371-1
56-Pin Plastic TSSOP Type II	-40 °C to +85 °C	74ABT16821ADGG	SOT364-1
56-Pin Plastic TSSOP Type II	-40 °C to +85 °C	74ABTH16821ADGG	SOT364-1

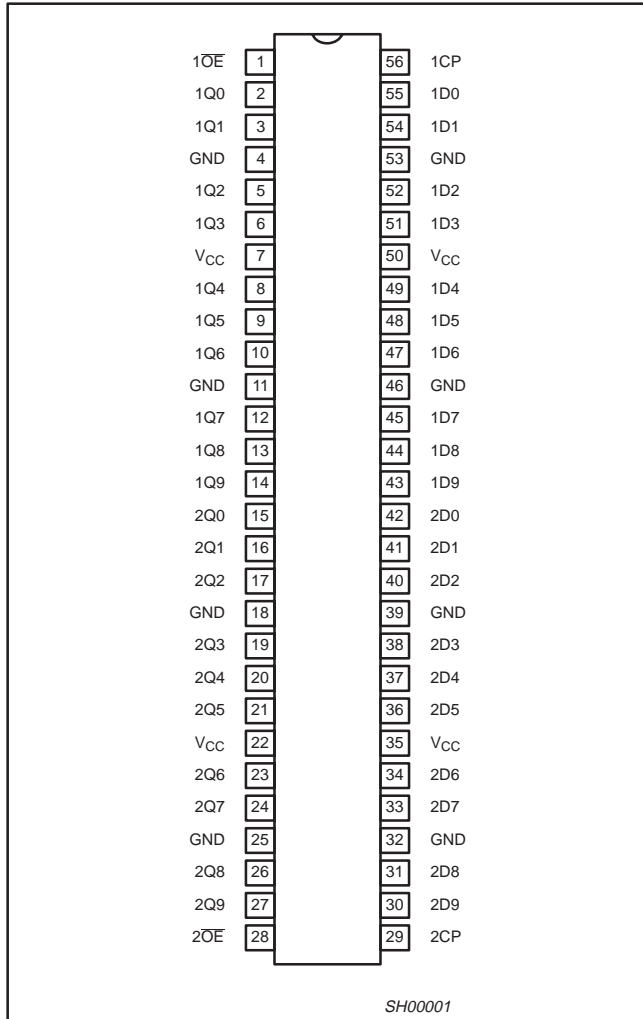
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 – 1D9 2D0 – 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
1, 28	1OE, 2OE	Output enable inputs (active-LOW)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

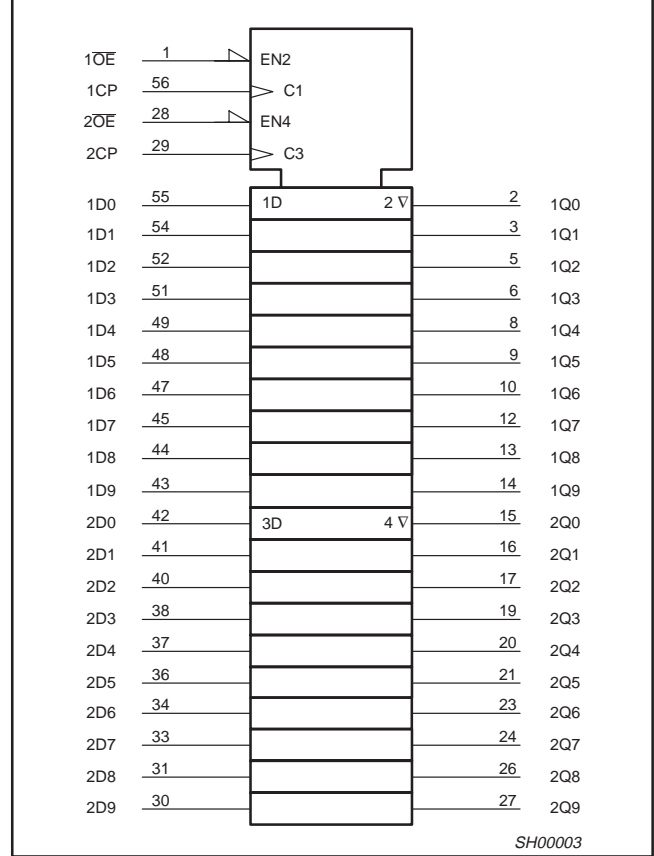
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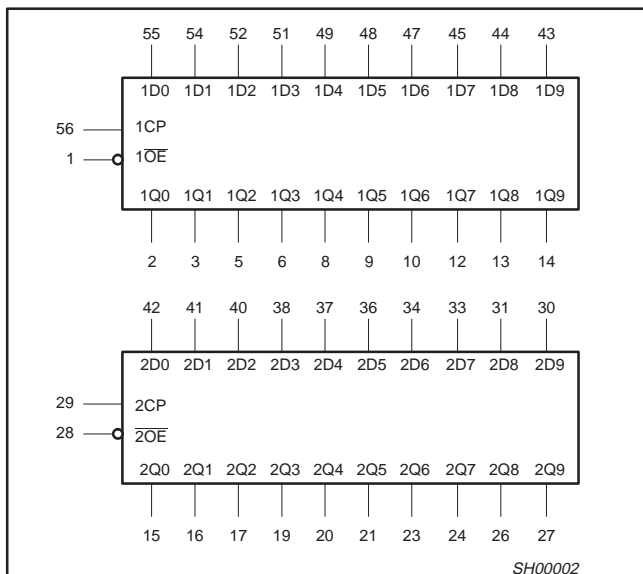
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

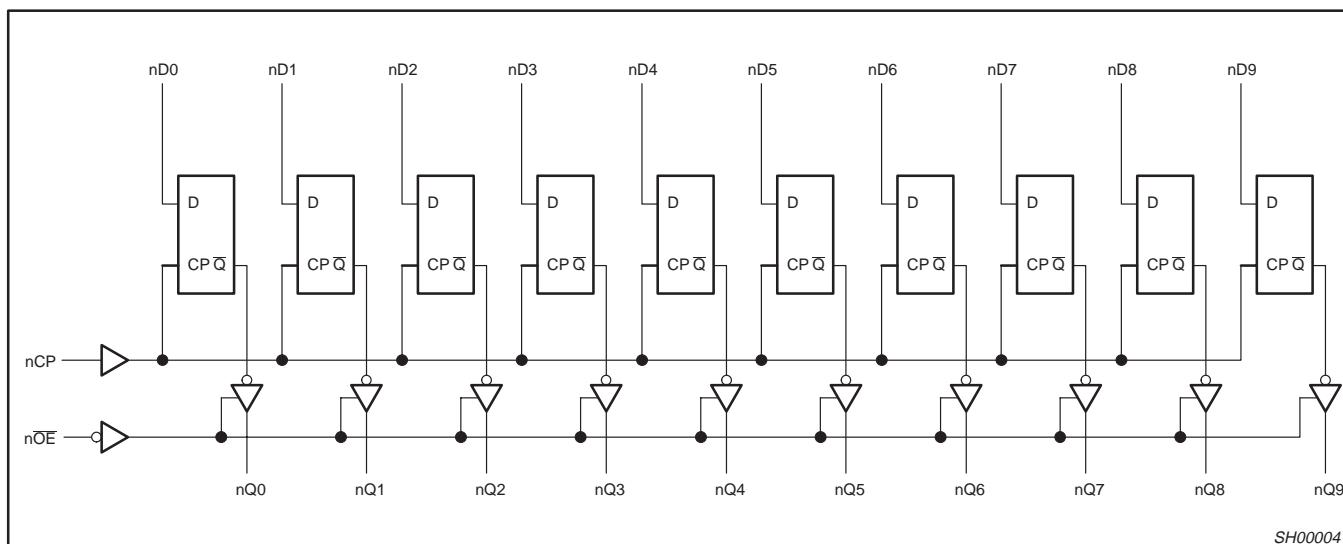
INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nCP	nDx		nQ0 – nQ9	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↑	X	NC	NC	Hold
H	↑	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

- H = High voltage level
- h = High voltage level one set-up time prior to the LOW-to-HIGH clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the LOW-to-HIGH clock transition
- NC = No change
- X = Don't care
- Z = High impedance "off" state
- ↑ = LOW-to-HIGH clock transition
- ↑ = Not a LOW-to-HIGH clock transition

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LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or HIGH state	-0.5 to +5.5	V
I_{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	-64	
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT	
			T _{amb} = +25 °C			T _{amb} = -40 °C to +85 °C			
			Min	Typ	Max	Min	Max		
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA		-0.9	-1.2		-1.2	V	
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V	
		V _{CC} = 5.0 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V	
		V _{CC} = 4.5 V; I _{OH} = -32 mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V	
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}		0.36	0.55		0.55	V	
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5 V; I _O = 1 mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V	
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND		±0.01	±1.0		±1.0	μA	
I _I	Input leakage current 74ABTH16821A	V _{CC} = 5.5 V; V _I = V _{CC} or GND	Control pins		±0.01	±1		±1	μA
		V _{CC} = 5.5 V; V _I = V _{CC}	Data pins		0.01	1		1	μA
		V _{CC} = 5.5 V; V _I = 0			-1	-3		-5	μA
I _{HOLD}	Bus Hold current inputs ⁵ 74ABTH16821A	V _{CC} = 4.5 V; V _I = 0.8 V		35		35		μA	
		V _{CC} = 4.5 V; V _I = 2.0 V		-75		-75			
		V _{CC} = 5.5 V; V _I = 0 to 5.5 V		±800					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V		±5.0	±100		±100	μA	
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1 V; V _O = 0.5 V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA	
I _{OZH}	3-State output HIGH current	V _{CC} = 5.5 V; V _O = 2.7 V; V _I = V _{IL} or V _{IH}		1.0	10		10	μA	
I _{OZL}	3-State output LOW current	V _{CC} = 5.5 V; V _O = 0.5 V; V _I = V _{IL} or V _{IH}		-1.0	-10		-10	μA	
I _{CEX}	Output HIGH leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}		5.0	50		50	μA	
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V	-50	-90	-180	-50	-180	mA	
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs HIGH, V _I = GND or V _{CC}		0.5	1		1	mA	
I _{CCL}		V _{CC} = 5.5 V; Outputs LOW, V _I = GND or V _{CC}		10	19		19	mA	
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}		0.5	1		1	mA	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND		0.25	1.5		1.5	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V a transition time of up to 100 μsec is permitted.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

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AC CHARACTERISTICS

GND = 0 V, $t_R = t_F = 2.5$ ns, $C_L = 50$ pF, $R_L = 500$ Ω

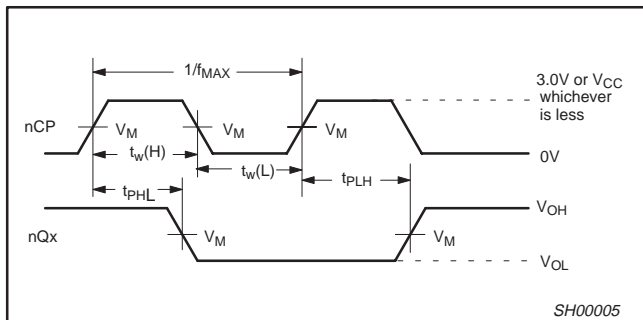
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{amb} = +25$ °C $V_{CC} = +5.0$ V			$T_{amb} = -40$ °C to $+85$ °C $V_{CC} = +5.0$ V ± 0.5 V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	160	250		160		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.3 1.1	2.4 2.0	3.3 2.6	1.3 1.1	3.7 3.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	3 4	1.4 1.2	2.5 2.3	3.3 3.0	1.4 1.2	4.1 3.7	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	3 4	1.6 1.3	3.2 2.3	4.1 3.1	1.6 1.3	4.8 3.3	ns

AC SETUP REQUIREMENTS

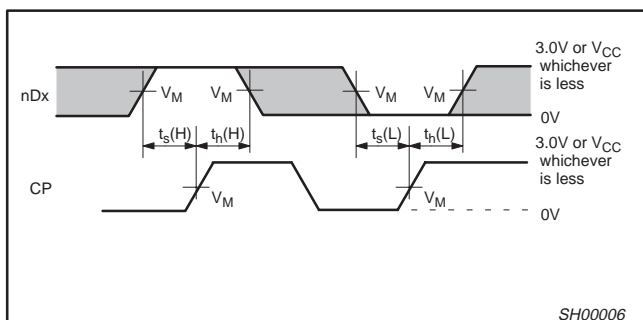
GND = 0V, $t_R = t_F = 2.5$ ns, $C_L = 50$ pF, $R_L = 500$ Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$T_{amb} = +25$ °C $V_{CC} = +5.0$ V		$T_{amb} = -40$ °C to $+85$ °C $V_{CC} = +5.0$ V ± 0.5 V		
			MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW nDx to nCP	2	1.8 1.8	1.2 -0.9	1.8 1.8		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW nDx to nCP	2	1.0 1.0	0.8 -1.0	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	nCP pulse width HIGH or LOW	1	2.5 2.5	0.8 1.0	2.5 2.5		ns

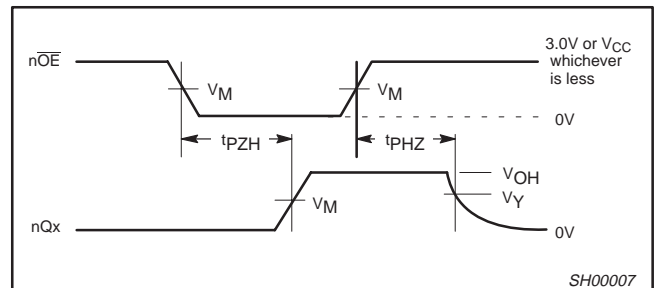
AC WAVEFORMS



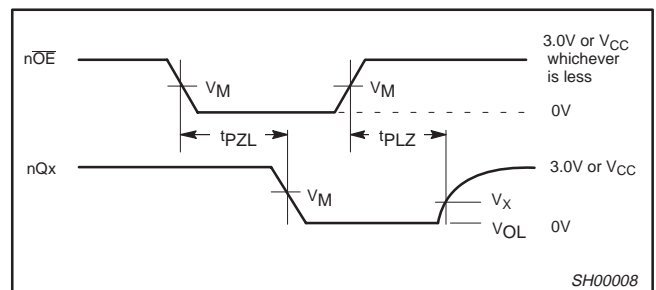
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock frequency



Waveform 2. Data Set-up and Hold Times



Waveform 3. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

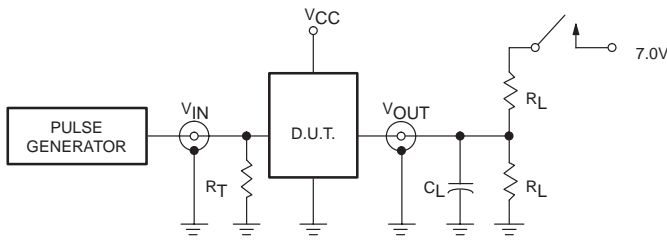


Waveform 4. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

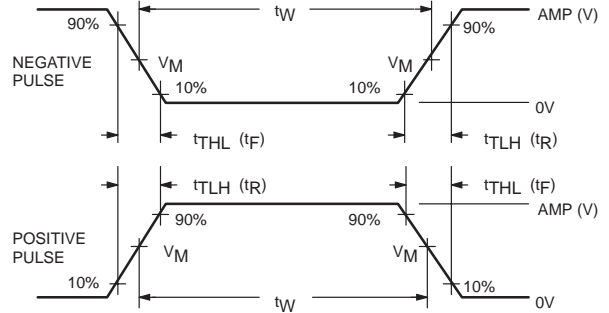
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TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{pZL}	closed
All other	open

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

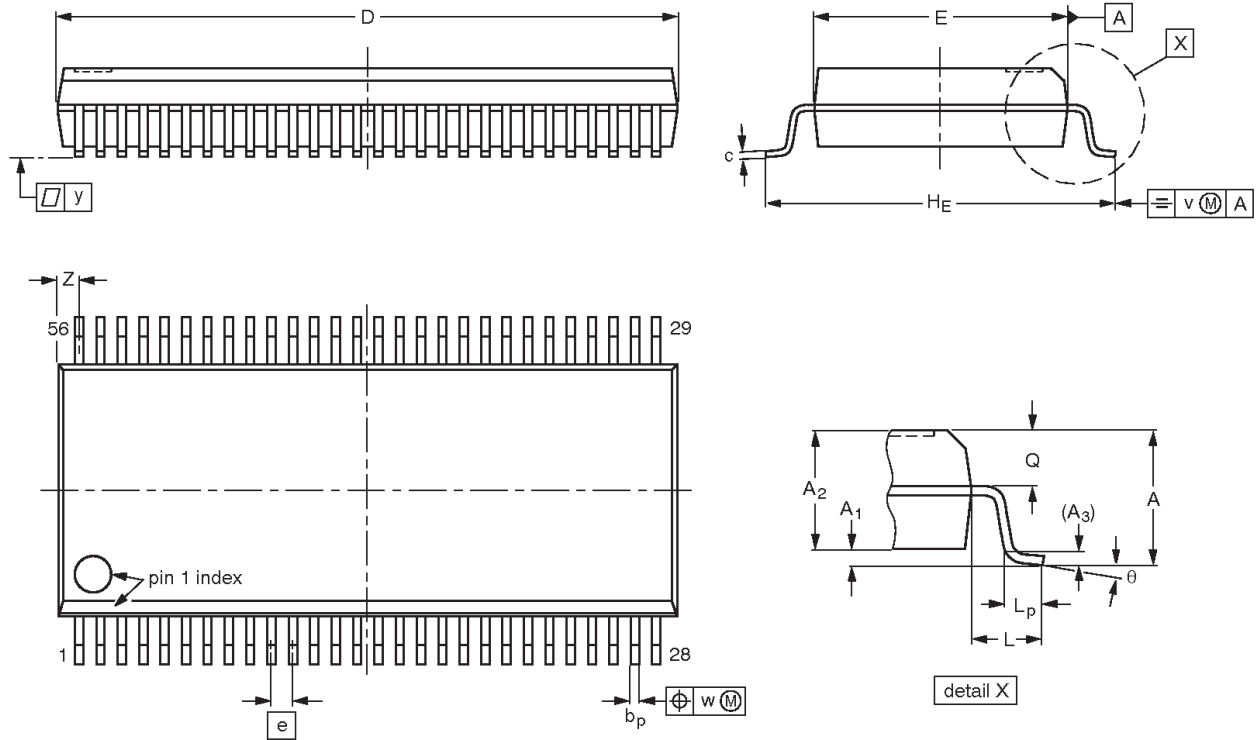
SA00018

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

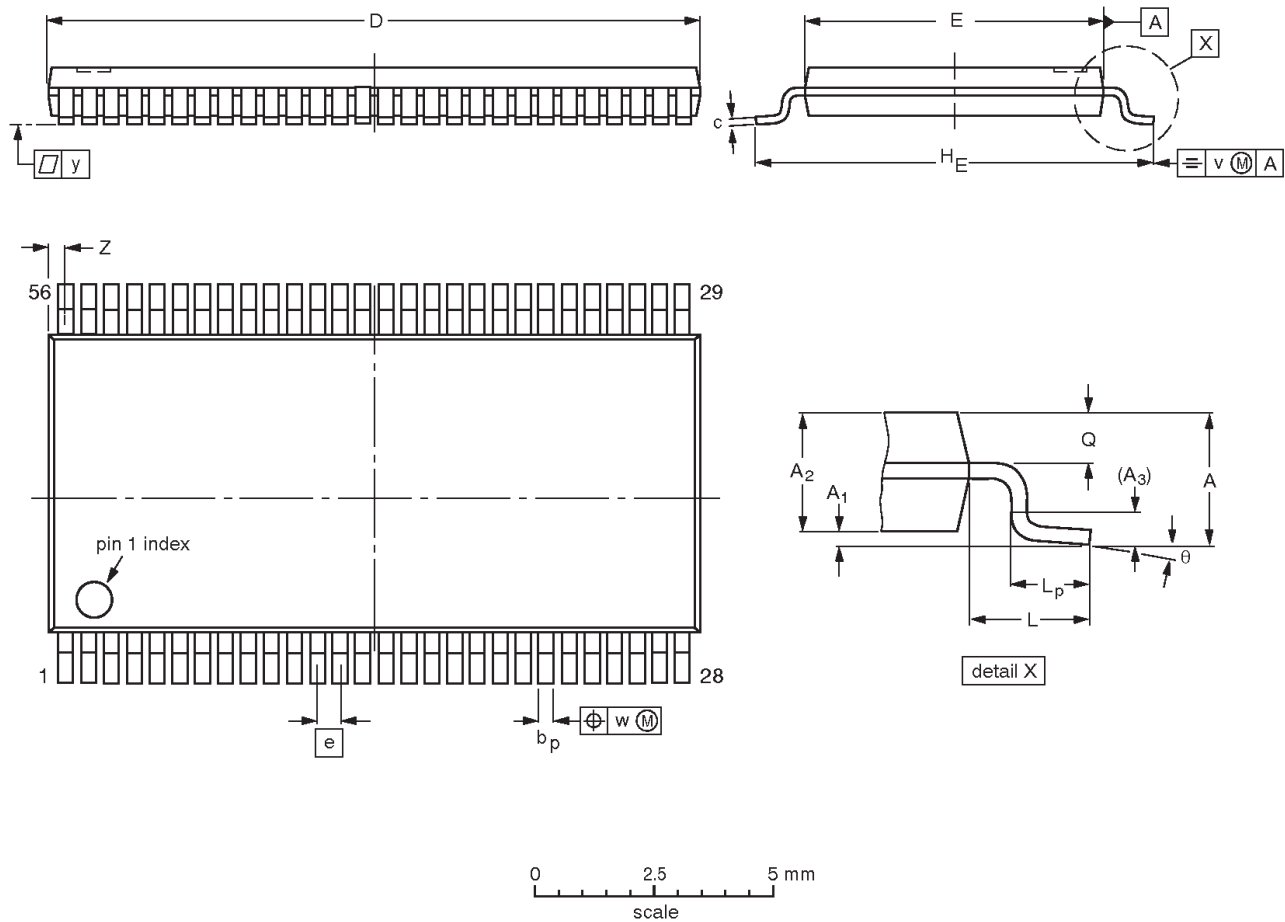
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				95-02-04 99-12-27

20-bit bus-interface D-type flip-flop;
positive-edge trigger (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153				95-02-10 99-12-27

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REVISION HISTORY

Rev	Date	Description
_2	20021213	Product data (9397 750 10855); ECN 853-1796 29295 of 12 December 2002. Supersedes data of 27 February 1998 (9397 750 03501). Modifications: <ul style="list-style-type: none">● Ordering information table: remove "North America" column; remove 74ABTH16821ADL package offering.
_	19980227	Product specification (9397 750 03501). ECN 853-1796 19026 of 27 February 1998.

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Document order number:

9397 750 10855

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