



Hot plug techniques with P82B96

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July 28, 2008 – update of 2003 slides



These slides are intended only to raise awareness of some of the issues that can require consideration in I2C hot-swap applications. There can be other significant issues and it is impossible to cover every possibility.

I never believed that the 'pre-charge' of an I2C bus was of any value during hot-swap and slide 7 gives some arguments against.

Pre-charge was shown in slide 2 only for completeness and because others were pushing it at that time.

In certain buffers pre-charge has been used to guarantee floating module bus lines are held in the logic LOW state. That is a separate consideration, it is not ideal for minimizing main bus glitches.

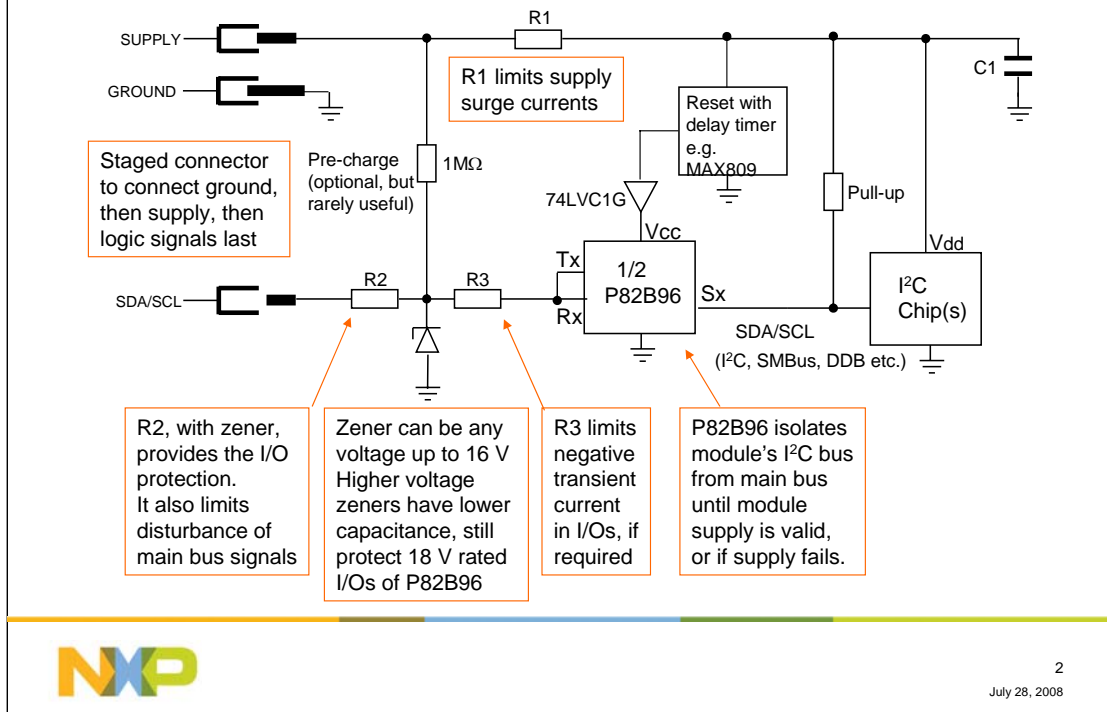
Personally I believe that for I2C using any of our cable drive methods there will not be problems created by the physical plug-in of modules but there always can be software problems caused by devices receiving partial I2C messages.

It's always possible, if customers are VERY demanding about the way hot-plug must be handled as far as possible by HARDWARE, to use the 'stop' detection in available buffers like PCA9511A and to 'AND' their READY signal into the supply-switching control of P82B96 or PCA9600 as shown in slide 2.

Since these slides were written in 2003 there are more resources to help customers with related applications, particularly where the main bus becomes a long cable instead of a backplane:

- a) There are two new App notes about driving cables. AN10658 and AN10710.
- b) PCA9600 has addressed the tolerancing issue of the Sx voltage level compatibility with low voltage logic or TTL.
- c) For a short cable around 2 m , even with 22 modules, possibly PCA9508s with additional ESD protection if required would be adequate.
- d) The P82B485 for differential drive to replace the P82B96 or PCA9600 used with a CAN driver to drive balanced signals.

Protecting a hot-plug module and the bus signals



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This slide shows a module that will be hot-plugged to a main or backplane bus as shown at the left side. (Only one bus logic signal is shown, the components on the other bus signal line will be identical).

Consider firstly the protection of the module itself.

- The pins must be protected against ESD. The level of protection depends on the application and the environment. The I/Os of P82B96 already pass ESD testing to 3500 V. For increased protection a zener is used. If it has a high voltage rating R2 can help limit the peak zener current. Strictly the zener can't prevent negative transient currents in the protection diodes (to ground) on the P82B96 I/Os but just a very small value resistor R3 will limit those currents to a safe value. R3 will only rarely be fitted in cases where extreme ESD is expected and would be in the range 2.2 to 10 ohms.
- When the logic pins of the module connect to the main bus their stray capacitance must be charged to the voltage on the main bus at that instant. That causes transients on the main bus. When the main bus has capacitance that is much greater than the added module pins then there will be no problems (see later slide). Precharge is not required and R2 can be just a low value around 100 - 330 ohms depending on the main pull on the backplane bus.
- The I²C chips on the module will have requirements on the state of the bus lines as the power to the chips increases from zero to its correct value. The usual requirement is that the bus lines must not be held low while the supply is being applied. They should rise at the same rate as the supply rises. If they were immediately connected to the external bus there is a chance that external bus will be low because it is carrying messages. If the P82B96 has no supplies it keeps all its I/Os open circuit. The pull-up on the local bus can then ensure the connected chips SDA/SCL signals rise with the power rail. A conventional Reset IC such as MAX809 can be used to monitor the local supply rail and its output will remain Low until the local supply has passed the rated threshold value. The MAX809 also includes a delay timer that holds the output Low for a further 240 milliseconds to allow the supply to reach its final value. The surge-limiting resistor R1 together with the filter capacitor C1 should be chosen to ensure the supply rises to the safe design value within the 240 ms delay timer period. When the supply is valid for 240 ms the MAX809 output will go High and the Pico gate buffer 74LVC1G will provide Vcc to the P82B96, activating it and providing a (buffered) connection between the main bus and the local bus chips.
- Note that this simple circuit does not provide any control of the instant that the local bus is joined to the main bus. It is preferable to make the connection when the main bus is idle. This will be discussed in another slide.
- While P82B96 is guaranteed to release all its I/Os when its supply fails, typically to a value around 1.4 V, it is guaranteed to be operational for 2 V on Vcc so it (alone) does not provide protection for a 5 V supply that falls to some voltage between 5 V and 1.5 V. The MAX809 monitoring the supply provides protection and disconnection in this case of 'brown out' or partial failure of the supply

Protecting a hot-plug module and the bus signals

- some possible requirements

- ▶ Module

- ESD protection
- Correct power-up and reset procedure
- Recovery procedure in case of a chip lock-up
- Logic voltage level shifting

- ▶ Main bus

- No glitches high or low when module is connected
 - Applicable to the supply rail as well as the bus logic lines
- Identifying when a new module is connected
- Recovery procedure if a module is removed while reading data from it
- Auto-disconnect of a faulty module (e.g. if holding bus lines low)



Protecting a hot-plug module - ESD

- ▶ The Standard for testing ESD immunity of equipment is IEC/EN 61000-4-2
 - Level 4 test voltages are 8 kV 'contact' and 15 kV 'air discharge' but equipment is available for testing to at least 30 kV and some suppressors are rated to 30 kV.
 - ESD testing of ICs is less severe, comparable to 'contact' tests with 1/5 the peak currents.
- ▶ Suppressor devices mostly do not clamp ESD pulses below IC data sheet limit voltage ratings
 - 5 V logic is usually protected by 6.8 V zeners that typically clamp to around 10 V.
- ▶ P82B96 I/Os pass IC tests to 3.5 kV without additional protection, are rated to 18 V, and their Tx/Rx breakdown voltage is typically above 45 V
 - Zeners / transient suppressors rated up to 16 V (clamping to around 30 V) can protect them.
 - 16 V zeners have much lower capacitance than lower voltage zeners. BZX84-C16 parts have 20 pF effective capacitance. (Measured by their effect on a 5 V bus rise time)
 - Zeners below 7V5 need to be low leakage types to prevent clamping the logic signals. PLVA656A (5V6) is low leakage but it loads a 5 V bus with about 75 pF.
 - Suppressors like BZA408B are rated for use on 5V logic lines and >15 kV ESD tests. They are actually bi-directional 6.8 V zeners. Their effective capacitance is about 40 pF.
 - Littelfuse SP0502BA are 6.8 V zeners with around 30 pF and rated to 30 kV in ESD tests.
- ▶ Balance ESD protection levels against bus capacitance overhead for the protection !
 - Consider 10x sink capability of P82B96 to lower the bus impedance and drive at least 4 nF
- ▶ Placement of the protection components greatly influences the immunity achieved



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A new range of ESD suppression products is available that is based on the series connection of a fast, low capacitance, diode and a zener diode. They are generally described as 'ultra low capacitance transient suppressors' or in similar terms.

If those products are measured, as they are rated, using zero volts dc bias and using a 1 MHz RF capacitance bridge they will indeed exhibit a very low capacitance reading – very much lower than the capacitance of their low voltage zener diode component.

When such diodes are used on a I2C bus their 'effective' capacitance (that is the effect they will have on bus rise time) is not so easy to determine.

When the voltage across such a device is increased from zero to the bus working voltage the zener diode's capacitance must be charged via the (conducting) series diode. In that case the effective capacitance will be the zener diode's capacitance. For a 5 V suppressor device with a rating around 1 pF that could be 100 pF or even much more. The zener capacitance, and its effect on a bus rising (for the first time) from 0 V to the nominal bus voltage, could be measured by shorting the device, applying a pull-up resistor to the supply, releasing the short, and observing the first exponential rise time.

If the device was shorted again, and before the zener capacitance has discharged released again, it may well also exhibit a low capacitance. Its equivalent is essentially a diode connected to a reference supply voltage.

The difficulty with applying such devices on an I2C bus is that the discharge time (or leakage current) of the zener will not specified so it is impossible to know whether the effect on I2C bus rising edges in a message will resemble the 'first', and therefore high equivalent capacitance, charging of the zener capacitance or will be more like the subsequent low capacitance equivalent of a fast diode connected to a reference voltage (the charged zener capacitance).

The attractiveness of their often very substantial protection ratings is tempting, but especially in hot-plug applications the effective capacitance at first connection is most likely to be the very large, unspecified, one.

In other I2C systems those products probably can provide useful ESD protection because it's likely the zener component will remain charged to above at least half its breakdown rating for the duration of normal I2C data bus sequences. Just remember when calculating any discharge time that SDA can be low for at least 8x SCL cycles before it is required to rise.

Hot-plug module - Supply and reset

▶ When the module is connected its power rail takes time to rise to its correct value. Until the module supply reaches the level for guaranteed correct operation of the connected chips there will be requirements to be met.

▶ Some requirements are:

- Microcontrollers need to be held in their reset state.
- Some I²C chips require their SDA/SCL pins to rise with their rising supply voltage. I/Os must not be pulsed or held low. This requires them to be separated from the main bus because it may be active and pulsing low.
- Some Standard-mode I²C parts have diodes from SDA/SCL to their supply. To prevent the main bus being clamped low through these diodes will also require their SDA/SCL pins to be separated from the main I²C bus until their supply is valid.

▶ Corresponding solutions:

- Use a reset chip e.g. MAX809 to monitor the supply voltage level and reset Micros.
- A reset with delayed 'output valid' is useful, it allows time for the supply to fully stabilize after crossing the reset's reference level. If the Micro contains integrated supply monitoring and reset then the P82B96 Vcc could be supplied/controlled by a port line.
- Use the 'supply valid' signal to power P82B96 (Buffer with a 74LVCxx gate if necessary.) P82B96 releases all its I/Os when its supply is removed (or falls below 1 V).



Main bus - supply and logic signal disturbance

- ▶ When the module is connected it must charge its on-board supply bypass and filter capacitors. Usually a small series resistor is sufficient to avoid disturbance to the main supply.
- ▶ When the logic supply pins make connection the main bus must charge the capacitance of these lines to the voltage level on the main bus.

There are many combinations of possible states at the instant of mechanical contact:

- The main bus lines are inactive, held high by pull-ups.
- The main bus is active and the bus lines are held low by an IC.
- The module supply/ground/logic pins connect in random order.
- The connector has pins arranged to cause a defined order of connection. Then the module bus lines may be pre-charged to the V_{cc} voltage, otherwise they will be low.

Objective:

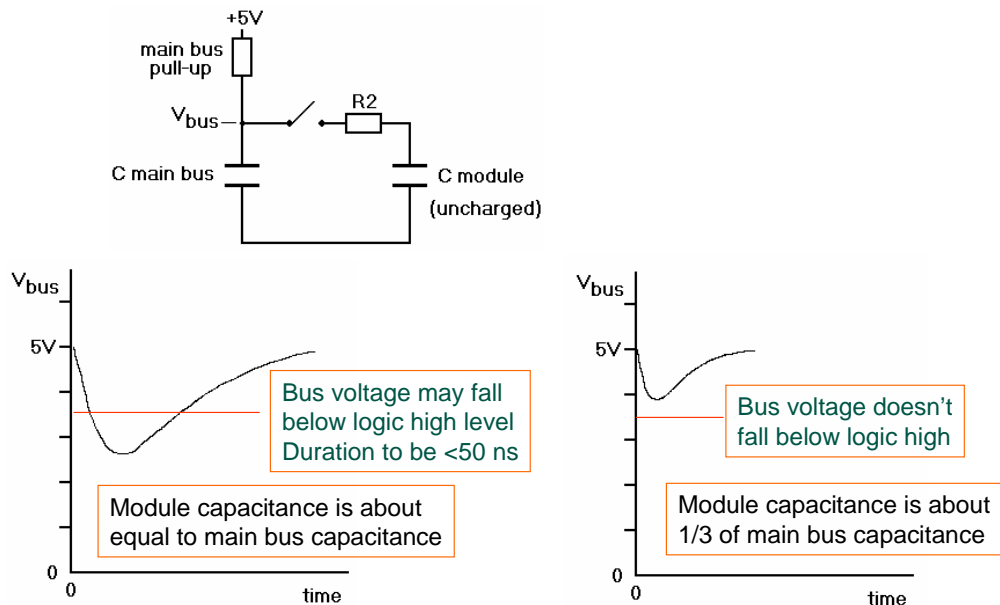
- Ensure any transient changes of the main bus logic state are shorter than 50 ns.

Strategies:

- Where possible try to arrange to connect modules when the main bus is inactive.
- Use a bus buffer with low input capacitance to isolate the module bus and its ICs.
- Minimize stray capacitance (**incl. ESD protection**) on module's main bus input terminals.
- Keep the capacitance of each module less than the main bus capacitance.



Equivalent circuit - module being connected to main bus



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To fully represent the distributed resistance/inductance/capacitance components of an I2C bus, or modules to be attached to it, is usually not practical so various simplified equivalent circuits are proposed. These will be more or less valid depending on the frequency components of the waveforms they are used to model. This treatment simplifies the equivalent circuit of the ICs and wiring, for high frequencies, to a lumped capacitance and ignores distributed inductance because it attempts to show the change in charge (and therefore voltage) on those ICs and the wiring capacitance that represent the main bus. The inclusion of inductive components will introduce transients/ringing but it is assumed their frequency components will be too high to cause logic voltage levels to be disturbed for as long as 50 ns. When the bus wiring between connection nodes exceeds, say, 1 meter then modeling as a transmission line would be more appropriate but the outcome will be similar.

This slide illustrates the school physics problem of calculating what happens when a charged capacitor is connected to an uncharged one. If there was no pull-up resistor the final voltage on the capacitors is calculated using the principle of charge conservation. The original total charge ($C \times V$) on the bus capacitor is shared between the capacitors in the ratio of their capacitances and their final voltages are equal.

So, for no bus pull-up, if the module capacitance was equal to the main bus capacitance, and the main bus was charged to 5 V, then after joining the module the joined bus voltage would be 2.5 V. When there is a pull-up the bus voltage does not fall so low, and it recovers with a time constant calculated from the final total bus capacitance.

In the first waveform drawing the module capacitance is assumed equal to the main bus capacitance. In this case there is a 'glitch' on the main bus down to almost half-rail (depends on the value of R_2 , the smaller the value of R_2 the lower the bus voltage will dip). In theory, for $R_2=0$ the bus dips to half rail.

In the second drawing the module capacitance is assumed 1/3 of the main bus capacitance. Again in theory, for a very small R_2 the bus will dip to $5 \text{ V} \times 3/4 = 3.75 \text{ V}$. That causes no disturbance of the logic high level. As R_2 is increased the bus dip becomes even less.

Conclusion: Keep the added module capacitance less than 1/3 of the bus it will be connected to and then there will be no significant disturbance to the main bus. If necessary add some capacitors to the main bus. Remember P82B96 can sink 10 times the normal I2C currents allowing lower pull-ups to be used and increasing the allowable bus capacitance to 4 nF.

Notice that the concept of pre-charging the module capacitance to V_{cc} will really only be useful in unusual cases where the module capacitance is greater than the bus capacitance it will be plugged onto, AND it is not possible to select the pull-up and R_2 to keep the transient duration below 50ns.

Hot-plug module - Control of logic signals

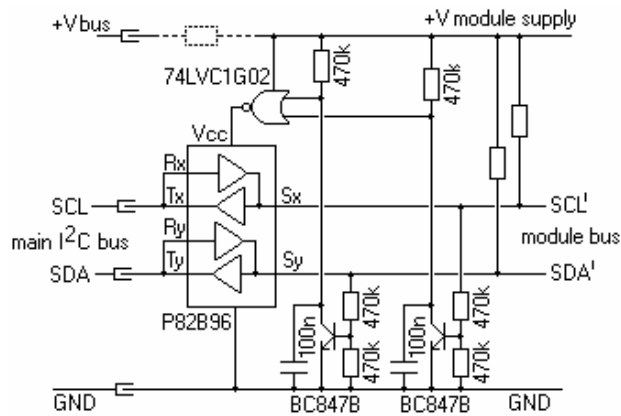
- ▶ **Even if a module is isolated until after its supply becomes valid it needs additional control.**
- ▶ Consider these possibilities:
 - System needs to know when a module has been added/removed.
 - Module may be removed while it is communicating.
 - Connection to the main bus may happen during a communication on the main bus.
 - Component failure may cause bus lines to be shorted and remain 'low'.
- ▶ Corresponding solutions:
 - Use software polling of the addresses of expected slave ICs. Modules with master capability can send an identifying message.
 - Bus master can identify a missing 'acknowledge' when writing to a slave, but when reading from a slave there is no ACK from the slave. In this case the master needs to re-address the slave and confirm it still provides an ACK.
 - Add bus logic detection of the main bus signals and delay the application of P82B96 supply until 1) supply is stable and 2) a 'stop' condition is detected.
 - Use 'bus low' detector with timing limit to remove P82B96 supply and disconnect the local bus.



Timed disconnect if bus line held low - example

If either module bus line remains low the corresponding 100 nF capacitor can charge and a gate input will become 'high' causing P82B96 V_{CC} supply to become 0 V and disconnect main bus lines.

Combine this function with supply sensing and delay circuit



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This circuit is intended to free the main bus on the left side if some component on the module bus holds either of the SCL'/SDA' lines low for a period set by the 100nF capacitor and 470k pull-up resistor.

Normally the bus lines only pulse low for short times. Every time they go high again the 100nF capacitor is quickly discharged by the transistor to 0V. If it is not discharged (by the bus line going high) within about 50 milliseconds then the V_{CC} supply to P82B96 will be removed and all its I/O lines are released, releasing the main bus.

(This circuit is not intended to function correctly if the main bus lines are stuck low. In fact it will cause low frequency oscillations on the corresponding module bus line(s) if they are held low. When the main bus is repaired it would be good practice to send a software reset sequence to all modules.)

When the module supply voltage exceeds the capability of standard logic gates then a low cost alternative is to use 'logic transistors' or Resistor Equipped Transistors (RETs) to switch V_{CC} to P82B96. AN255-02 has examples.

The example shown is valid for modules that have full multi-master capability in the system and is therefore more complex than required in simpler single master systems

While all slave devices must have the capability to drive the SDA line low to acknowledge or send data, only few, relatively rare, slave devices will have a driver on their SCL line. The exceptions will be slaves that require 'clock stretching' capability, which is rare today, and microcontrollers used as slaves that simply allocate open drain ports to generate the I2C signals.

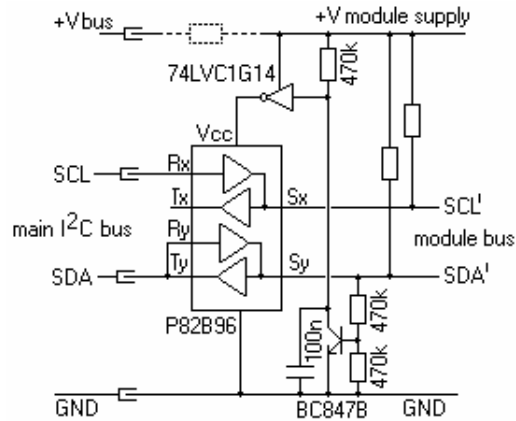
When there are no slave devices on the module that have SCL drivers a simpler/better alternative is possible. The components for sensing of Sx can be removed and the Rx pin (i.e. the SCL buffer input) tied to V_{CC} instead of to Tx. That makes the SCL buffer unidirectional and allows the main bus master to attempt bus recovery routines that require clocking of the slaves SCL. When those software recovery routines succeed and SDA becomes free again this arrangement will also return to normal operation.

Timed disconnect if bus line held low - preferred arrangement in applications with only slaves on the module

If there are no master devices on the module, and no slaves requiring clock stretch capability, then the SCL buffer is wired to be unidirectional by disconnecting Tx.

This allows the master to attempt stuck-bus recovery routines.

Combine this function with supply sensing and delay circuit



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This circuit is intended to free the main bus on the left side if some component on the module bus holds the SDA' line low for a period set by the 100nF capacitor and 470k pull-up resistor.

Normally the bus lines only pulse low for short times. Every time they go high again the 100nF capacitor is quickly discharged by the transistor to 0V. If the capacitor is not discharged (by the bus line going high) within about 50 milliseconds then the Vcc supply to P82B96 will be removed and all its I/O lines are released, releasing the main bus.

(This circuit is not intended to function correctly if the main bus SDA is stuck low. In fact it will cause low frequency oscillations on the SDA module bus line if it is held low. When the main bus is repaired it would be good practice to send a software reset sequence to all modules.)

When the module supply voltage exceeds the capability of standard logic gates then a low cost alternative is to use 'logic transistors' or Resistor Equipped Transistors (RETs) to switch Vcc to P82B96. AN255-02 has examples.

The general example in the previous slide was valid for modules that have full multi-master capability in the system and is therefore more complex than required in simpler single master systems

While all slave devices must have the capability to drive the SDA line low to acknowledge or send data, only few, relatively rare, slave devices will have a driver on their SCL line. The exceptions will be slaves that require 'clock stretching' capability, which is rare today, and microcontrollers used as slaves that simply allocate open drain ports to generate the I2C signals.

When there are no slave devices on the module that have SCL drivers then this simpler/better alternative is possible. The components for sensing of Sx can be removed and only the Rx pin (i.e. the SCL buffer input) is connected to the main bus. Tx is left open circuit. That makes the SCL buffer unidirectional and allows the main bus master to attempt bus recovery routines that require clocking of the slaves SCL. When those software recovery routines succeed and SDA becomes free again this arrangement will also return to normal operation.

